AD-A058 506 POWER ELECTRONICS ASSOCIATES INC FAIRVIEW PARK OH F/G 9/5
ADVANCED POWER PROCESSING TECHNIQUES FOR DC TO DC CONVERTERS.(U)
AUG 78 F C SCHWARZ DAAB07-74-C-0568
UNCLASSIFIED DELET-74-0568-F NL

1 OF 2
AD
A058506

LEVEL II

A025915

Research and Development Technical Report

DELET-74-0568-F

ADVANCED POWER PROCESSING TECHNIQUES FOR DC TO DC CONVERTERS

Francisc C. Schwarz

POWER ELECTRONICS ASSOCIATES, INC.
24532 Lorain Road
North Olmsted, OH 44070

August 1978

Final Report for Period 1 July 1974 - 29 December 1977

DISTRIBUTION STATEMENT

Approved for public release; distribution unlimited

Prepared for:
Electronics Technology & Devices Laboratory

ERADCOM

US ARMY ELECTRONICS RESEARCH AND DEVELOPMENT COMMAND
FORT MONMOUTH, NEW JERSEY 07703

NOTICES

Disclaimers

The citation of trade names and names of manufacturers in this report is not to be construed as official Government indorsement or approval of commercial products or services referenced herein.

Disposition

Destroy this report when it is no longer needed. Do not return it to the originator.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: DELET-74-0568-F	2. GOVT ACCESSION NO. / 3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): Advanced Power Processing Techniques for DC to DC Converters	5. TYPE OF REPORT & PERIOD COVERED: Final Report, 1 July 1974 to 29 Dec 1977 / 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): Francisc C. Schwarz	8. CONTRACT OR GRANT NUMBER(s): DAAB07-74-C-0568
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Power Electronics Associates, Inc., 24532 Lorain Road, North Olmsted, OH 44070	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 1L1 62705AH94 P4-294
11. CONTROLLING OFFICE NAME AND ADDRESS: US Army Electronics Research & Development Command, ATTN: DELET-PE, Fort Monmouth, NJ 07703	12. REPORT DATE: August 1978 / 13. NUMBER OF PAGES: 111
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office): 1L162705AH94	15. SECURITY CLASS. (of this report): UNCLASSIFIED / 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited. 122 p. P4

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

DDC RECEIVED SEP 13 1978 F

18. SUPPLEMENTARY NOTES

for 1 for 2

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Power Processing Techniques, DC to DC Converter, Series Capacitor Inverter-Converter, Transistor Operated Series Converter, High Operating Frequency, Low Switching Losses, Low Electrical Stresses, Controlled Variable Anti-parallel Diode Conduction, Controlled Nonlinear Resonant Circuit

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The feasibility of efficient ultra light weight dc power supplies was investigated and confirmed. The results of this study were embodied in a 190 Watt model, which indicates a component density of 126 W/kg. Power was derived from a source with the range from 22 to 32 VDC. Four output channels provide ±5 VDC and ±15 VDC, respectively. Each output channel has the characteristic of a current source, is individually controlled and maintains a 0.1 percent static accuracy, independent of the loading, or overloading of any or all of the other output channels. The system was also shown to be short

(Cont on Reverse Side)

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

391 607

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

Item 20 - ABSTRACT - Continued

circuit proof at any and all of the output channels. The full power efficiency of the system was measured at 73.35 percent. This efficiency could be further improved with the use of power Litz wire throughout the system and with the availability of power components with suited terminals for the relatively high currents. No intrinsic barrier was found to a further increase of the internal frequency of 50 kHz with its significant higher harmonic content. Efficiencies in excess of 95 percent were attained at the 1 kW level at input/output voltages near 200 VDC and with the same internal converter frequencies.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. Program Summary.

1.1. Scope

The objective of this program was to investigate the feasibility of improvements of the technology of dc converters with ohmic isolation between the input and its voltage regulated output ports. Emphasis was placed on the:

1. improvement of their power density, expressed in kW/kg;

concurrent with an improved or unimpaired:

2. high efficiency of dc power conversion;

3. reliability of operation and

4. cost effectivness in terms of technical complexity and need for maintenance by qualified personnel.

Meeting of the first above listed goals was successfully attempted by concurrently:

5. performing the voltage scaling and stabilization operation in one single process |1|, and

6. raising the internal frequency of operation of the dc converter up to 50 kHz.

Reports on the successfull combined attainment of these two requirements could not be found in the literature except for substantially lower frequencies of operation (10 to 20 kHz) with the use of thyristors as switching elements |2,3,4,5|.

Feasibility of the use of transistors in converters with series resonant circuits at an internal frequency of 20 kHz was demonstrated in the first phase of this program when 100 Watts were derived from a 80 - 160 VDC source at 93 percent efficiency |6|.

A concurrent program which was conducted by this author yielded an efficiency of 95 percent when 1 kW was derived from a 220 VDC source by a converter of the same type with an internal frequency of 50 kHz |7|.

Both above cited cases involved single output channels of 200 VDC.

The second phase of this program which is the subject of this report, required four individually controlled output channels with voltages of ± 5 and ± 15 VDC, respectivly. Power was derived from a 22 - 32 VDC source, with a nominal value of 28 VDC.

An account of the methods which were used in the attempts to overcome the limitations of the state of the art is given in part 2. The thereto pertaining systems analysis is contained in part 3. Information on design and development is presented in part 4. The system test data are presented in section 5.1. and followed by a discussion in section 5.2.

1.2. Results.

Feasibility of converter operation with an internal frequency of 50 kHz was demonstrated. The therefrom derived improvement of power density near 80 W/kg in packaged form could be indicated. All functional objectives, concerning static stability in the form of closely controlled output voltages within 0.1 percent were attained. Short circuit capability of the individual channels was demonstrated and proved not to interfere with the accuracy of maintaining the required output voltages of the other channels within the prescribed tolerances. Attainment of the other goals, such as insensitivity to source "noise" or audio susceptibility, operation within the desired ambient temperature range and reliability could be indicated. The full power efficiency of the system of 73.35% could be improved with the use of power Litz wire throughout the system, with emphasis on the wirewound magnetic components; further improvement could be attained with the availability of power components with better suited terminals.

1.3. Summary Conclusions.

The feasibility of ultra light weight dc power supplies with internal frequencies of 50 kHz in an electrically rugged form appears demonstrated with completion of the here presented work. Power densities of packaged equipment of 50 W/kg appear to fall well within reach of reality, after a component power density of 126 W/kg has been demonstrated with the work, presented in this report and embodied in the supplied breadboard. Further work on the parallel operation of independently controlled loads with the use of series resonant circuits and the development of improved joining techniques could yield further improvements of the here described technology. Limitations for a further increase of the internal frequencies of dc converters are not discernible at this time.

2. Purpose

The objectives of this program were to answer the questions whether it is feasible to:

1. Increase the internal frequency of dc converters to 50 kHz without impairment of the efficiencies which are customary at lower frequencies, such as 20 kHz |2,3|;
2. Retain a reasonable proportion of the advancements of the recently developed technology of transistorized inverter-converters, employing series resonant circuits for power transfer and control |6,7|.

The above cited requirements were compounded by:

3. lowering of the input voltage from a previous nominal value of ~ 130 to 28 VDC;
4. requiring individual control of four (4) output channels;
5. lowering of the output voltage from a previous nominal value of 200 VDC to 5 and 15 VDC, respectivly.

2.1. Summary Results of the Preceeding Program Phase

The inherent limitations of the commonly used parallel inverter-converter were explained in sections 2.1.1. and 2.1.2. of the First Interim Report (FIR), prepared under this program |6|. These limitations prevent an

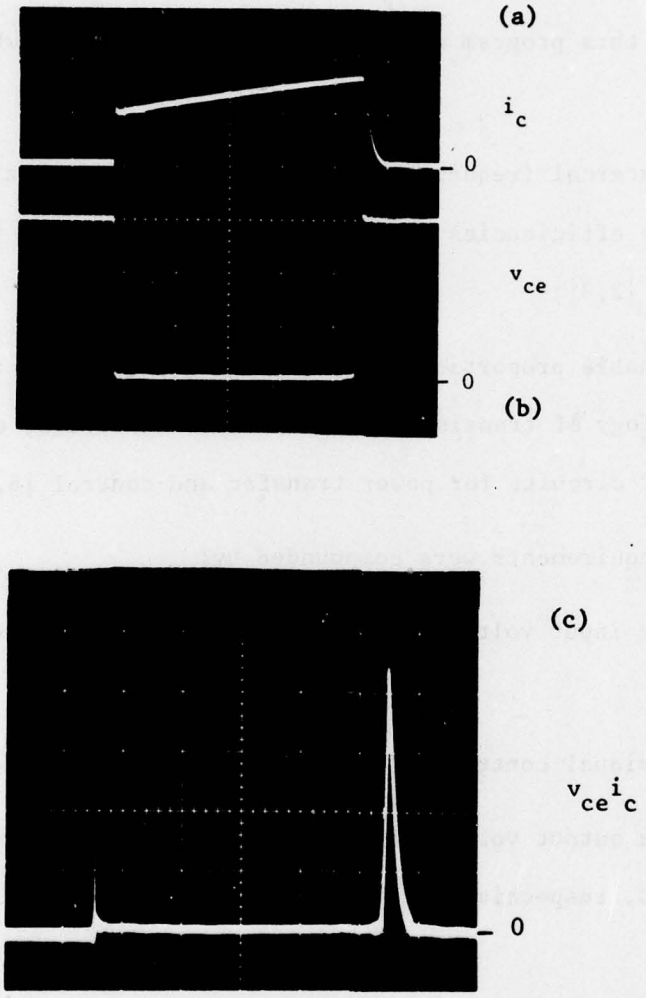

Figure 2.1.

Waveforms of a switched transistor: (a) the collector current i_c; (b) the collector voltage v_{ce}; (c) the power dissipation in the collector circuit $v_{ce}i_c$.

efficient attainment of frequencies beyond 10 kHz, and even then exclude simultaneous achievement of voltage scaling and output voltage stabilization by one single process of pulse modulation.

This limitation is rooted in the power dissipation which occurs in the power transistor during its phases of transition from the nonconducting to the conducting state and vice versa. The own difficulties with which the transistor struggles under these conditions to regroup the space charges near its base junction within a very short time interval is compounded by the parasitic characteristics of the transformer, the therewith associated conductors, and by the interacting semiconductor devices of the output rectifier |8|.

It has been shown that the therefrom resulting dissipation in the power transistor is due to: a fixed component, caused by the transistor's voltage drop during settled current flow from its collector to emitter; and a frequency dependent component which is caused by the number of switching events per second |9|.

The causes of the power dissipation in the transistor are illustrated in the oscilloscope curve traces shown in figures 2.1.(a),(b) and (c), which appear self-explanatory. The significant effects of the above explained dissipation process in the form of power spikes which coincide in time with

the leading and the trailing edge of the transistor's current pulse are clearly discernible in figure 2.1.(c) and support the concerned statement contained in the preceeding paragraph.

The above named power spikes are all, but completely removed in the dc converter, employing series resonant circuits for power transfer |2,3,6,7,9|. A simplified schematic of the one half bridge configuration of the primary power circuit of the transistorized version of this type of converter is shown in figure 2.2. Its mode of operation and its functional characteristics are documented in the preceeding FIR and in the literature |2,7|.

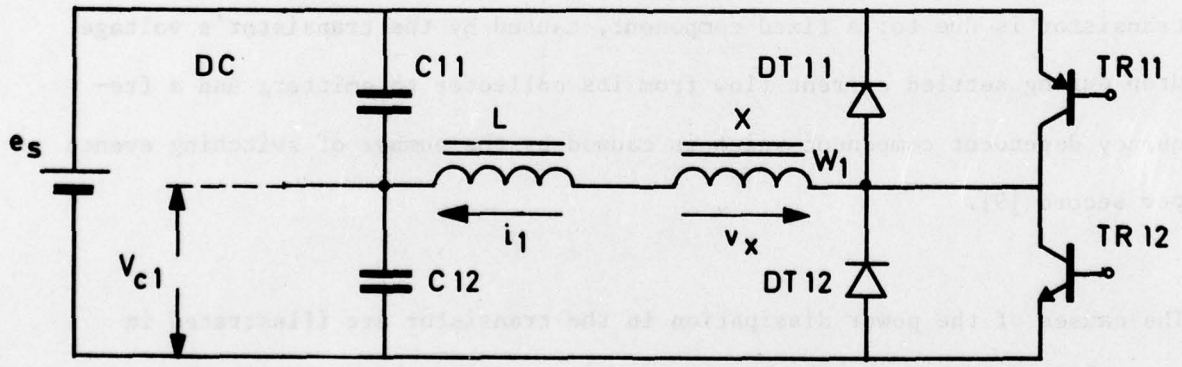

Figure 2.2. Primary circuit of half bridge series converter

The transistors are powered by individual proportional drives. Their junctions are thoroughly cleared after each interval on conduction of the resonant current. The combined result of (1) the inherent mechanism of switch operation in series resonant circuits, (2) the avoidance of "over-drive" by use of proportional drive techniques and (3) the carefull clearing of the transistor's junctions when the "antiparallel" diode prevents a significant collector to emitter voltage drop, is the attainment of an almost ideal switching characteristic of the transistors.

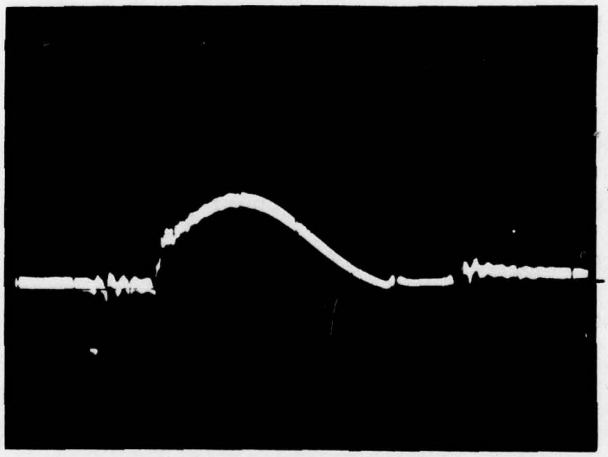

figure 2.3. Curve trace of the dissipation of one transistor in the series resonant circuit.

The effect of this favorable switching characteristic is clearly discernible in the photograph of the oscilloscope trace in figure 2.3. This trace shows the v_{ce} i_c product across the switching transistor. The two power spikes of figure 2.1.(c) have disappeared; the v_{ce} i_c curve follows the collector current waveform. In summary it is concluded that the switching losses in the semiconductor elements are solely restricted to the conduction losses.

The efficiency of the switching devices is, therefore, independent of the frequency of the converter operation. To extend the verifications of this fact also to transistors in series resonant circuits was one of the most significant results of the preceeding phase.

Attainment of a favorable over all efficiency of 93 percent of the 100 Watt series capacitor converter at a favorable component power density of 125 W/kg supports the belief that this type of converter allows the construction of light weight equipment.

The short circuit capability of this type of converters was also demonstrated and verifies the substantial degree of protection which this sytem provides for the, otherwise, proverbially fragile power transistors. This short circuit capability is combined with another inherent property of this converter: the low ratio of maximum vs. average stress in the switching components which is evidenced by (1) the dissipation pattern shown in figure 2.3. and by the current self limiting properties of the system as a whole |2,5,6,7|.

2.2. Extension of the Internal Converter Frequency.

One of the significant objectives of this work was to verify that the converter frequency could be extended to the 50 kHz range without an inherent impairment of the converter's efficiency. This principle was proven on a parallel effort in which a 1 kW dc converter was operated with an efficiency of 95 percent at an internal frequency of 50 kHz |7|. An input voltage of 220 VDC was stepped down to 200 VDC for this purpose.

The results of the above referred to work appear to verify the expectation at the start of this program, that the losses in the switching transistors are virtually independent of their frequency of operation in resonant circuits. Expectation of this property was based on the absence of power peaks in the dissipation pattern of the switching transistors, as discussed with reference to figure 2.3.

This independence of switching losses from frequency is verified by the results of the here presented work: the switching losses seem to be well within the limits of theoretical-experimental analysis; the usual sizable increase of switching losses with increasing frequency is absent.

However, significant attention had to be paid to effects in wiring and in connectors. The relatively high frequency of inversion of 50 kHz, the therefrom

resulting filter frequency of 100 kHz and the therewith associated higher harmonics of several hundred kiloHertz brings the concerned frequency components near and within the range of radio frequencies. Techniques applied in radio engineering must be used to prevent the well known undesirable phenomena in wiring and connectors. This includes: careful subdivision of paths of current conduction in connecting wires, the windings of magnet-coils, and problems when joining with and in the single piece metallic connectors, such as at the terminals of component parts, including semi-conductor components.

The magnetic field patterns near ferreous cores seemed to be affected by the higher frequency; this was indicated by an increasing discrepancy between the calculated and actually measured inductance in fabricated inductors.

Capacitors were another area of concern which, however, did not materialize.

2.3. Operation of Several Individually Controlled Loads.

The objectives of the effort, as reported here, were to operate several loads in parallel from a low voltage source and to provide low voltage outputs for equipment containing electronic logic. These objectives characterize the discussed converter as pertaining into a different category in which relatively high currents are used to process a moderate

volume of power. The power losses in any converter systems are governed by the processed current and by the ratio of the sum of the voltage drops in the path of the processed current vs. the input or output voltage, as appropriately interpreted for that purpose.

This is illustrated as follows: Let all voltage drops in the switching elements in the path of power current transfer be viewed from a 5 VDC output channel and assume a power transformer step down ratio of roughly 3:1. Assume a voltage drop of 0.5 in each of the output rectifier Schottky barrier diodes and assume a 1 VDC drop for each of the two of each pair of transistors in the primary circuit. If all semiconductor voltage drops are reflected into the 5 VDC channel there their sum

$$v_{sem5} \simeq 0.5 + 2/3 \simeq 1.16 \qquad (2.1)$$

The maximum possible efffciency η_{max} of the system is limited to

$$\eta_{max} < v_{o1}/(v_{o1} + v_{sem5}) = 5/6.16 \simeq 0.812 \qquad (2.2)$$

where

v_{o1} = 5 VDC, the dc voltage of one of the 5 Volt output channels.

That is, not counting all other losses in the magnetics, the wiring and the connectors. It was, fortunately, possible to

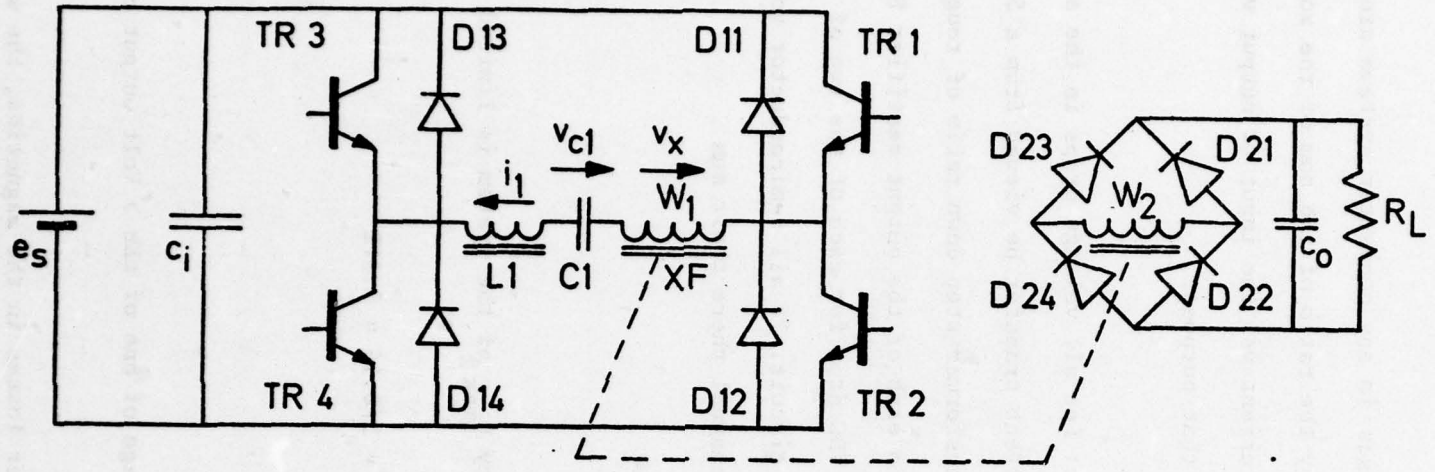

Figure 2.4. Full bridge configuration of the transistorized converter employing series resonant circuits.

obtain a reasonable efficiency within the given constraints. The above argument is made to illustrate one of the significant characteristics of the here described task.

It was, above, tacitly assumed that a full bridge converter configuration be used, as indicated in figure 2.4. This choice was made in order to accomodate the limited current carrying capability of fast switching transistors, such as the TRW SVT 50-30 for a peak collector current of 30A. The full bridge configuration of the converter utilizes all of the source voltage e_s, rather than to be restricted to one half, as is the case in the one half bridge configuration.

Each of the four output channels required individual voltage control in order to meet the requirements of the Technical Guidelines. This was, originally, intended to be implemented with one single output transformer, as discussed in parts 3 and 4 of this presentation. This approach was eventually abandoned, when faced with serious problems which are rooted in the physical limitations of components. Another approach was, eventually, implemented as explained in subsection 3.2.2.

The "main" channel with an output of + 15 VDC had to maintain a static

stability of ± 0,5%. The other "secundary" channels were allowed to vary 2% from their average nominal output voltage. A classical problem of the series capacitor inverter-converter surfaced when it appeared impractical to continue with the single transformer approach with parallel output channels. This problem was solved as presented in subsection 3.2.2.

2.4. System Control Requirements.

2.4.1. The Protection System.

The primary new requirement for the protection system appeares as the need to attain the completion of the processing of signals which allows inception of each succeeding half cycle for the purpose of continuation of the converter operation, within less than 2 μsec. This time limit is imposed by the necessity to leave at least 8μsec. for the duration of the transistor current in order to retain a reasonably low current form factor ρ_i for the purpose of attaining a favorable over all efficiency |2|.

A "turn around time" of 2 μsec, as explained above, required the implementation of a number of individual steps in the converter's logic mechanism. This is discussed with reference to figure 2.5.

(1) A current zero crossing detector ascertains the existence of an approaching condition in which the resonant current will cross through its level with

a given polarity of its di_1/dt and

(2) sends an inhibiting signal to one of the shown AND gates to terminate

(3) the drive for the concerned power transistors who's collector current is near of becoming zero;

(4) the resulting signal flow is processed by the transformer ST.

(5) The base drive is, accordingly, terminated and

(6) the remaining charge is removed from the transistor's base junctions.

(7) A signal is generated in one of the windings of the transformers JT

(8) and transmitted to one of the trigger terminals of the Bistable Multivibrator,

(9) which, in turn, changes state and thus

(10) energizes the opposite AND gate.

(11) This gate energizes the respective transformer ST, which then

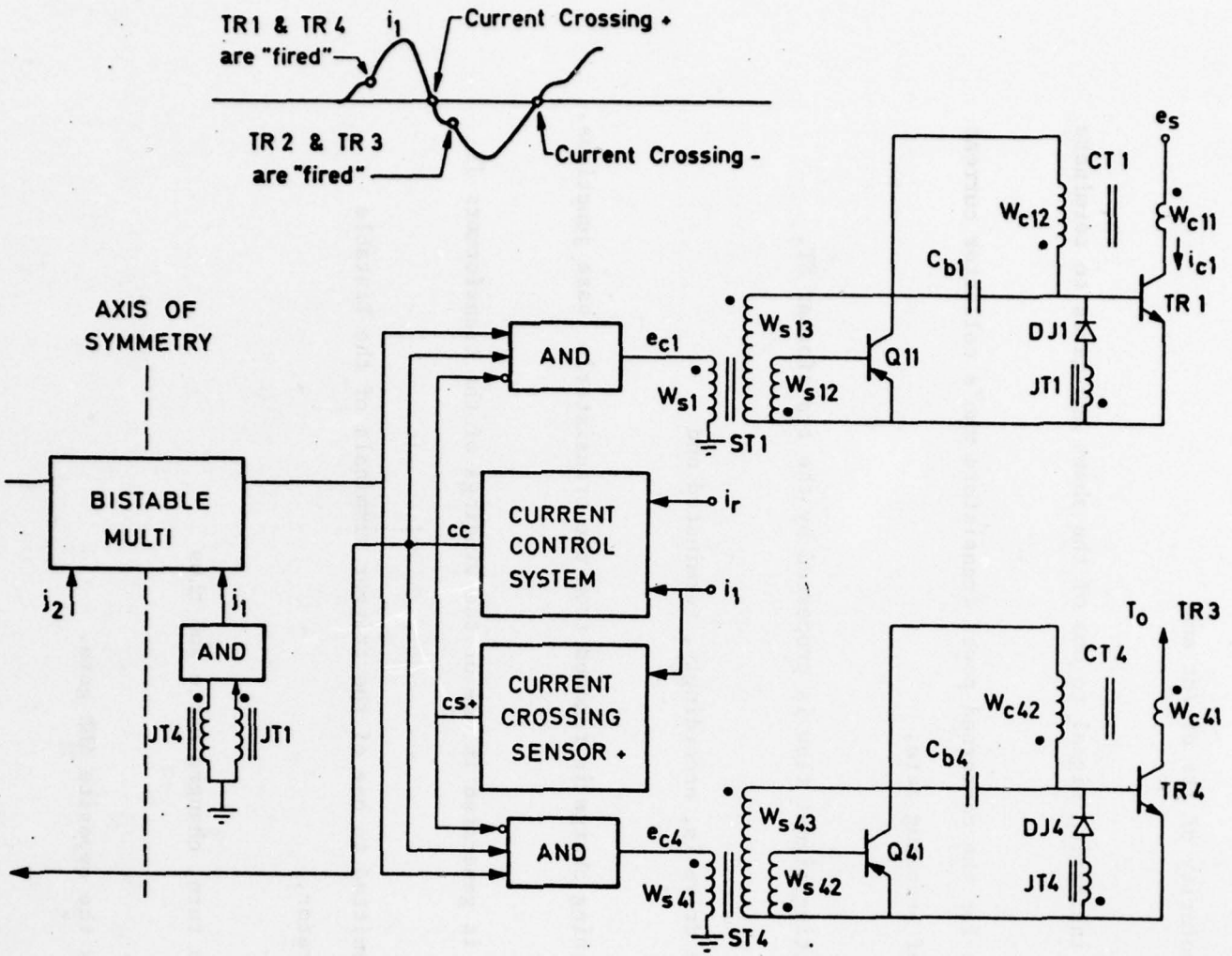

Figure 2.5. Simplified circuit and block diagram of the converter's electronic control and protection system.

(12) energizes the base of its power transistor.

Each of the above listed twelve staps requires a certain time interval; their sum cannot be more than 2 μsec. The degree of difficulty is illustrated by the fact that step (6) indicating clearing of the base junctions requires in itself ~0.5 sec., thus leaving ~1.5 sec. for the other eleven steps. The transfer of powerful signals in the order of 1 A current through transformers ST involves the leakage inductances of these magnetic devices which cause appeciable time delays. Thus most signal processing operations have to be completed within 100 nsec. or less, a demanding task for noise insensitive logic with built in sizable precantionary threshold levels and burdened with power comsumption limitations.

In the light of the above explained requirements it was necessary to abandon the former electronic protection systems design which was developed for thyristor operation not higher than 20 kKz with a "turn around time" of not less that 5 sec. A substantially faster protection system had to be developed; its interaction with the power system is treated in subsection 3.2.2.

2.4.2. Control of Four Independent Output Channels.-

Control of the four individual output channess in accordance with the requirement stated in section 2.3. is implemented by providing each individual channel

with a separate control mechanism.

The mechanization of the above stated principle and its interface with the power system are treated in subsection 3.3.3.

3. System Analysis.

3.1. Analysis of the Full Bridge Configuration.

The full bridge version of the series capacitor dc. converter will be used for this part of the program. The system behavior is identical with that of the half bridge configuration of the same converter used in the previous phase of the program |6|. A simplified schematic of the primary power circuit is shown in figure 2.4. The functional aspects of full bridge operation have been verified. Each pair of transistors TR1 - TR4 and TR2 - TR3, respectively carries the resonant current i_1. This current has an analogous characteristic as the one in the half bridge configuration. This is explained in the FIRST TECHNICAL INTERIM REPORT of April 1976, prepared under the same program. All other quantitative relations used throughout this program apply, except for the fact that now

$$q = v_2/e_s; \quad v_2 = v_{xa} \tag{3.1}$$

rather than $2v_2/e_s$ used before. The transformer "sees" now the entire source voltage e_s instead of its former Thevenin equivalent $e_s' = e_s/2$.

The voltage $v_{c1}(t_k)$ of capacitor C_1 at the end of one half cycle of the resonant current i_1 has to be such that it exceeds

$$v_{c1}(t_k) > e_s + v_2 \qquad (3.2)$$

in order that the capacitor C_1 be able to drive a charge through the antiparallel diodes D11 and D14 and the transformer against the source e_s.

The largest net voltage $v_{xa\ max}$ that could be "seen" by the primary winding W_1 of transformer XF is

$$v_{xa\ max} = e_{s\ min} - 2v_{ce\ max} \qquad (3.3)$$

where

$v_{ce\ max}$ = the average voltage drop over the individual transistors during conduction of the maximum average current.

For the required minimum source voltage $e_{s\ min}$ = 22 V and an expected average transistor voltage drop of 1 V is

$$v_{xa\ max} = 20\ V \tag{3.4}$$

However, the actual transformer voltage amplitude v_{xa} must be smaller than $v_{xa\ max}$ in order that the circuit remain in a state of oscillation. This smaller voltage $v_{xa} = v_2$ is established by calculation of the parameter q defined in relation (3.1).

The initial voltage $v_L(t_k)$ over the series inductor L_1 is given by

$$v_L(t_k) = e_s - v_{c1}(t_k) - v_2/\eta \tag{3.5}$$

where

η = efficiency of the converter |2|.

For the formulation of (3.5) it is assumed that all of the charge emanating from the source of energy with voltage e_s passes through the primary winding W_1 of the power transformer; thus all leakage currents through transistors TR i and Diodes D1i (i = 1, 2, 3, 4) are neglected. It is then assumed that all power losses caused by the inefficiency of the system manifest

themselves in form of an apparent increase of the voltage v_2 of the load, as reflected into the primary circuit of the converter system. A voltage drop

$$i_{1av}R_s = v_2(1 - \eta)/\eta \tag{3.6}$$

reduces the average value v_{Lav} of v_L during each cycle, if all power losses in the system are thought of as being caused by an apparent series resistance R_s. The therefrom resulting voltage drop reduces the "net driving voltage" $v_L(t_k)$ of the series resonant circuit and is therefore incorporated in the term v_2/η in (3.5). Voltage

$$v_{c2} = v_{c2}(t_k) + \frac{1}{C_2}\int_{t_k}^{t} (i - i_{1av})dt \tag{3.7}$$

where

C_2 = the output filter capacitor as reflected into the primary converter circuit; v_{c2} is the voltage of C_2.

Figure 3.1 illustrates the discussed significant waveforms [2,6].

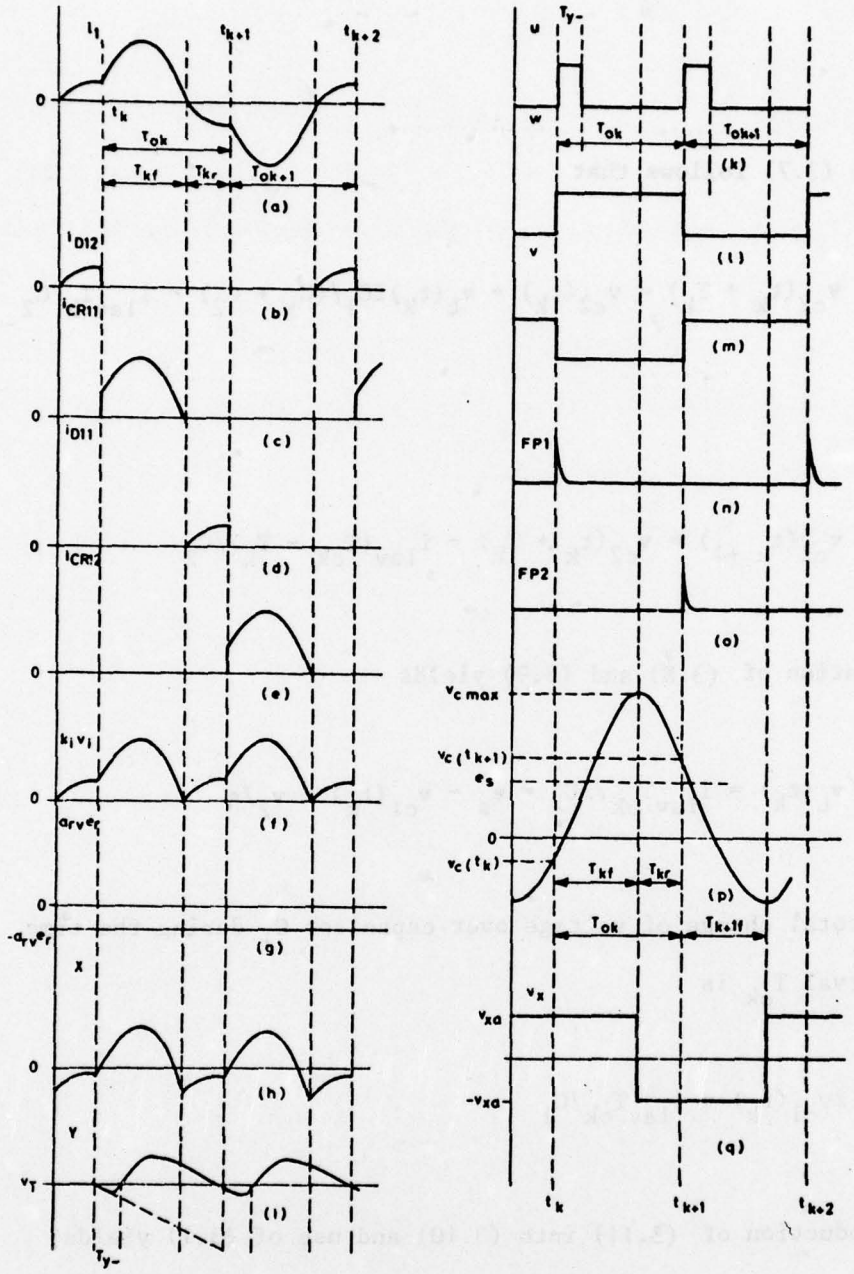

Figure 3.1.

The significant waveforms of the resonant circuits.

From (3.7) follows that

$$v_{c2}(t_k + T_k) = v_{c2}(t_k) + v_L(t_k)2C_1/(C_1 + C_2) - i_{1av}T_k/C_2 \quad (3.8)$$

and

$$v_{c2}(t_{k+1}) = v_{c2}(t_k + T_k) - i_{1av}(T_{ok} - T_k)/C_2 \quad (3.9)$$

Summation of (3.8) and (3.9) yields

$$v_L(t_k) = i_{1av}T_{ok}/2C_2 = e_s - v_{c1}(t_k) - v_2/n \quad (3.10)$$

The total change of voltage over capacitor C_1 during the time interval T_{ok} is

$$2v_{c1}(t_k) = i_{1av}T_{ok}/C_1 \quad (3.11)$$

Introduction of (3.11) into (3.10) and use of (3.1) yields

$$q = n\{1 - (v_{c1}(t_k)/e_s)(C_1/C_2)\} \quad (3.12)$$

Capacitor C_2 is calculated in the following manner. First, the difference

$$r_{pp}' = v_{c2\ max} - v_{c2\ min} \tag{3.13}$$

is defined and derived from relation (3.7). Then the peak to peak ripple r_{pp}' is normalized with respect to the average voltage v_2 of capacitor C_2 so that

$$r_{pp}/V_o = r_{pp}'/v_2 = 0.211\ i_{1av}T_{ok}/C_2v_2 \tag{3.14}$$

where

r_{pp} = the peak to peak ripple superimposed on the output voltage V_o.

Relation (3.14) holds for the immediate succession of half sinusoids of current. The term 0.211 must be removed in the limiting case when $i_{1av}/i_{1av\ max} \to 0$.

For

$$C_1/C_2 = (0)10^{-2} \tag{3.15}$$

where

(0) = "the order of",

is according to (3.12) and the literature |2|,

$$q \lesssim \eta \tag{3.16}$$

The peak to peak voltage of capacitor C_1 is according to (3.2) governed by

$$v_{c1}(t_k)_{min} > 2e_{s\,min} = 44 \text{ V.} \tag{3.17}$$

For

$$i_{1av} = \tfrac{1}{2} i_{1av\,max} \tag{3.18}$$

when $\psi_r = \psi_{r\,max} = \pi$, follows for constant $e_s = e_{s\,min}$ |2| that

$$v_{c1}(t_k)_{max} \simeq 1.3\, v_{c1}(t_k)_{min} \text{ for } i_{1av} = \tfrac{1}{2} i_{1av\,max} \tag{3.19}$$

Voltage

$$v_{c1}(t_k)_{max} = (1.3)(44) = 57 \text{ V} \tag{3.20}$$

for $e_s = e_{s\,max} = 32$ V. Let then $v_{c1}(t_k)_{min} > 44$ V as given by (3.17) to secure satisfactory operation of the resonant circuit throughout its intended range of functioning. The range for $i_{1av} < \frac{1}{2} i_{1av\,max}$ involves a discontinuous state of current i_1 and does, therefore, not require further investigation because discontinuity of i_1 does not alter the waveform of the current appreciably during its resonating phases.

Use of (3.11) and (3.14) in (3.12) yields for $e_s = e_{s\,min}$

$$q_{max} = n\{1 - q(r_{pp}'/v_2)/2(0.211)\} \tag{3.21}$$

and thus

$$q_{max} = \frac{n}{1 + n(r_{pp}'/v_2)/(2)(0.211)} \tag{3.22}$$

The term 0.211 increases to 1 for $i_{1av} << i_{av\,max}$ as explained under (3.14) so that

$$q_{max} = \frac{0.8}{1 + (0.8)(0.005)} \simeq 0.8 \tag{3.23}$$

Following (3.1), the transformer voltage amplitude

$$v_2 = (0.8)(22) = 17.6 \text{ V} \tag{3.24}$$

A voltage

$$v_2 = 17 \text{ V} \tag{3.25}$$

is arbitrarily chosen to allow a margin of 1.5 V between the transformer voltage and the "net" source voltage

$$e_s' = e_s - 2v_{ce} - v_D' \simeq 18.5 \tag{3.26}$$

where

$$v_D' = (N_1/N_2)v_D \tag{3.27}$$

and

V_D = the voltage drop ($\sim$ 0.5 V) over the Schottky barrier diodes in the secondary power circuit;

N_i = the number of turns on the respective windings W_i of the power transformer XF.

The maximum average current in the primary circuit

$$i_{1av\ max} = 190/17 \simeq 11.2\ A \tag{3.28}$$

The rms current |2|

$$i_{1rms} = \rho_i i_{1av} \simeq (1.3)(11.2) = 14.6\ A_{rms} \tag{3.29}$$

Relations (3.11), (3.20) and (3.28) are used to calculate

$$C_1 = (11.2)(10^{-5})/114 \simeq 1\ \mu F \tag{3.30}$$

where

$f_i = (1/2T_{ok})$, the frequency of inversion of 50 kHz

Capacitor C_2 is found from (3.14):

$$C_2 = (11.2)(10^{-5})/(17)(0.005) \simeq 1.32 \text{ mF} \qquad (3.31)$$

The effective series capacitance

$$C \simeq 1 \quad \mu F \qquad (3.32)$$

The series inductance

$$L_1 = (T_o/\pi)^2/C = (8\ 10^{-6}/\pi)^2/10^{-6} \simeq 6.5\ \mu H \qquad (3.33)$$

where

$T_o = \pi\sqrt{LC_1} = 8\ 10^{-6}$, the half cycle duration of the series resonant circuit.

The steady state maximum peak current |2|

$$i_{1\ peak\ ss} \simeq 1.6\ i_{1av\ max} = 18 \text{ A} \qquad (3.34)$$

3.2. The Secondary Circuits.

3.2.1. The Initial Approach.

The secondary circuits of the converter are shown in figure 3.2. The $\pm$ 5 V output channels are fed from one of the center tapped

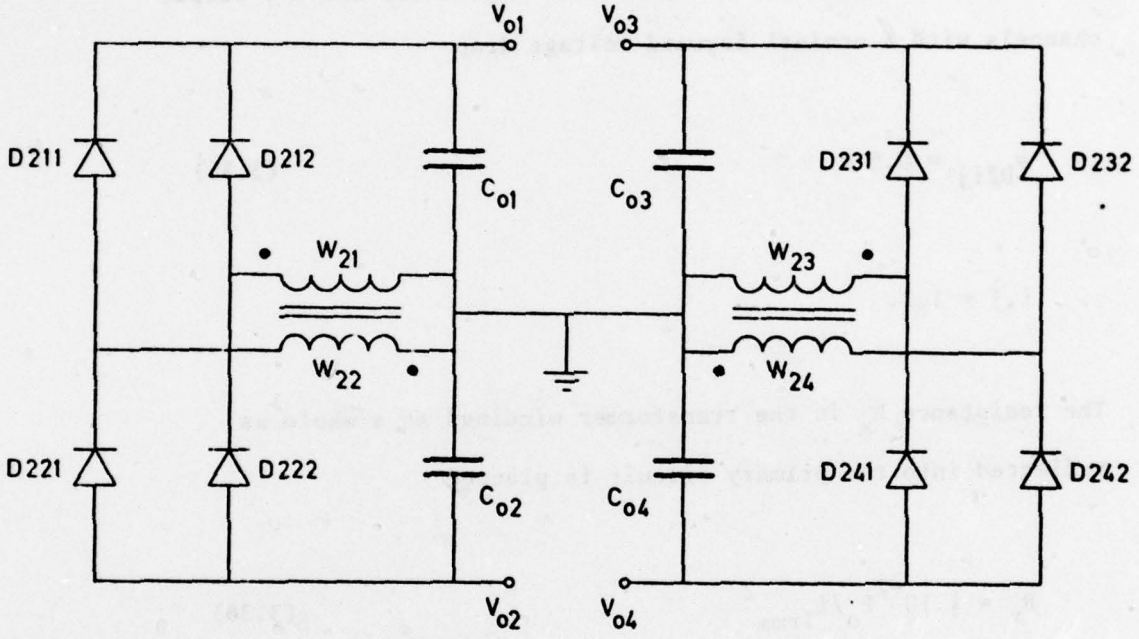

Figure 3.2.

The secondary power circuits of the power converter. First Approach.

transformer windings, with halves W_{21} and W_{22}. The $\pm$ 15 V output channels are fed from another of the center tapped transformer windings, with halves W_{23} and W_{24}.

It is intended to use Schottky barrier diodes for the 5 V output channels with a nominal forward voltage drop

$$v_{D2ij} = 0.5 \text{ V} \tag{3.35}$$

$$i,j = 1,2.$$

The resistance R_x in the transformer windings as a whole as reflected into the primary circuit is planned

$$R_x = \tfrac{1}{2}\, 10^{-2} P_o / i_{1rms}^{\,2} \tag{3.36}$$

It is, arbitrarily, assumed that the power losses are evenly divided between the magnetic and the electric circuit of the transformer XF. Thus

$$R_x = 10^{-2} 190/2\ 213 = 4.46\ 10^{-3} \text{ Ohm} \tag{3.37}$$

The cumulative full load current i_{212rms} in the windings W_{21} and W_{22} is given by

$$i_{212rms} = 14.6(100/190)(17/5) = 26.1 \text{ A} \tag{3.38}$$

with

$$i_{21\ rms} = i_{22\ rms} = 13.05 \text{ A} \tag{3.39}$$

for each of the windings W_{21} and W_{22}. The full load power loss in each of the windings is for a transformer efficiency $\eta_{XF}=0.44$, given by

$$P_{21} \simeq \tfrac{1}{2}0.01\tfrac{1}{2}190\tfrac{1}{2}100/190 \simeq 0.122 \text{ W} \tag{3.40}$$

The resistance in each of these windings is then given by

$$R_{x21} = R_{x22} = 0.122/169 = 0.72\ 10^{-3} \text{ Ohm} \tag{3.41}$$

The cumulative full load current i_{234rms} in windings W_3 and W_4 is given by

$$i_{234rms} = 14.6(90/190)(17/15) = 7.8 \text{ A} \tag{3.42}$$

with

$$i_{23rms} = i_{24rms} = 3.9 \text{ A} \tag{3.43}$$

for each of the windings W_{23} and W_{24}. The full load power loss P_{23} in each of these windings is given by

$$P_{23} \simeq \tfrac{1}{2}0.01\tfrac{1}{2}190\tfrac{1}{2}100/190 \simeq 0.110 \text{ W} \tag{3.44}$$

The resistance in each of these windings is given by

$$R_{x23} = R_{x24} = 0.110/15.2 = 7.2\ 10^{-3} \text{ Ohm} \tag{3.45}$$

The +15 V output channel will be feedback controlled to ascertain a deviation of no more than 0.5 % from its nominal value, as required. Discrepancy of the voltage between the four individual channels will occur if any pair of these is unequally loaded. If the "lead" channel for the +15 V output is fully loaded and its counterpart, the -15 V channel is only to 10 % loaded then the voltage differential

$$\Delta v_{234} = (0.9)(3)(7.2\ 10^{-3}) \simeq 19.5 \text{ mV} \tag{3.46}$$

or

$$10^2 \Delta v_{234}/v_{34} = (19.5\ 10^{-3}/15)10^2 = 0.13\ \% \qquad (3.47)$$

The maximum deviation of 0.13 % between the two 15 V output channels appears tolerable and leaves

$$(2 - 0.5 - 0.13) = 1.37\ \% \qquad (3.48)$$

tolerance for tracking of the rectifier diodes in these channels and of other causes of deviation of channel voltages.

Another case arises, when the +15 V "lead" channel is fully loaded and any of the 5 V channel is only to 10 % loaded. The voltage differential

$$\Delta v_{13} = (0.9)(10)(0.72\ 10^{-3}) = 6.48\ 10^{-3}\ V \qquad (3.49)$$

or

$$10^2 \Delta v_{13}/v_{12} = (6.48\ 10^{-3}/5)10^2 = 0.129\ \% \qquad (3.50)$$

This maximum deviation appears, again, tolerable and leaves, approximately, 1.37 % tolerance for tracking of the rectifier diodes and other causes of deviation of channel voltages from each other. The same holds, of course, true in the converse case if the +15 V channels were only lightly and any of the other channels were fully loaded.

The margin of approximately $\pm$ 1 % of 5 V, that is $\pm$ 50 mV should fall within the variation of voltage drop in the Schottky barrier diodes which will be selected for that purpose.

3.2.2. Limitations of the Single Transformer Approach.

Application of the above described systems concept for the independent control of four power output channels caused implementary problems which led to the application of an alternative approach.

Part of the report on the experimental aspects of this work, found in section 5, is preemted in order to present the reasons for following an alternative approach.

The problem originated in the fact that the needed, relatively large output filter capacitors C_{oi} could not accomodate the therewith associated 100 kHz ripple of the currents i_{zi} (i=1, 2, 3, 4). Relativly large capacitances in the order of millifarads appeared necessary to keep the effects of the sizable ripple currents within the prescribed output voltage ripple limitations. The need for millifarad size output filter capacitors emerges with equation (3.31) which identifies the reflected cumulative output filter capacitance $C_2 \approx 1.32$ mF at the 17 VDC level.

Non-electrolytic capacitors of mF size are too bulky for use in a system for which weight is at a high premium. Yet the higher quality Tantalum electrolytic capacitors of the General Electric KSR series proved not suited for the 100 kHz application at hand.

Operations of a number of parallel power output channels within a series capacitor converter via one single transformer is predicated on the availability of high quality filter capacitors with an almost negligible ripple voltage $|10|$. This condition could not be satisfied, as explained above. The ensuing problem is described with reference to figure 3.3.

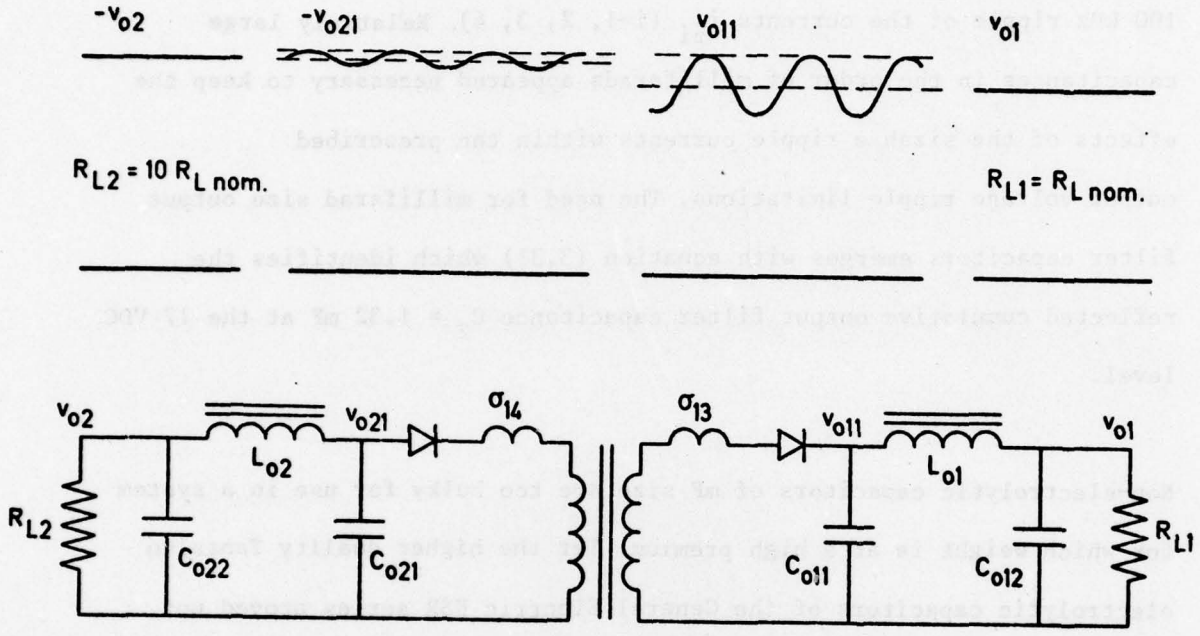

Figure 3.3.

Two output power channels with equal nominal output voltage of opposite polarity and with a 10:1 loading disparity.

Parts of the circuits of two, otherwise identical, output channels with opposite polarity are shown in figure 3.3. Each channel indicates only a one half wave rectification process for purpose of simplicity of presentation.

It is tacitly assumed that a full wave rectification process is implemented in each of the two channels through the addition of diodes, not shown in this figure. It is also assumed at this time that the filter inductances $L_{oi} = 0$ (i=1,2). Capacitors C_{o11} and C_{o12} then combine to one single capacitor C_{o1}; capacitor C_{o2} is thought of analogously.

If $R_{L2} = 10\ R_{L1}$ then channel No 1 is loaded ten times as heavily as channel No. 2, a ripple v_{rppo1} of the output voltage v_{o1} will ensue which is considerably larger than that of the output v_{o2}, such that

$$v_{rppo1} \simeq 10\ v_{rppo2}. \qquad (3.51)$$

It follows that the respective rectifier diodes establish conduction at different output voltage levels because of the difference in the magnitude of the ripple voltage at that moment. This difference is compounded by the existence of the leakage inductances $\sigma_{13} \neq \sigma_{14}$. Different amounts of energy would be stored in these leakage inductances even if $\sigma_{13} = \sigma_{14}$, not to speak of under the given conditions.

It follows that each of the output filter capacitors C_{oi} "sees" another average voltage being impressed by its associated transformer winding. Furthermore, even if the peak voltages

$$v_{o1\ peak} = v_{o2\ peak} \tag{3.52}$$

it would necessarily follow that

$$v_{o1\ av} \neq v_{o2\ av} \tag{3.53}$$

The above explained process which leads to the discrepancy (3.53) would not occur, if

$$\sigma_{13} = \sigma_{14} = 0 \tag{3.54}$$

and if

$$C_{o1} = C_{o2} \to \infty \tag{3.55}$$

It was explained in the introduction to this subsection that the shortcomings of electrolytic capacitors could not satisfy (3.55), or

represent any sizable value at a capacitor current frequency of 100 kHz. It was, furthermore, explained that "paper" capacitors of values in the order of millifarads are too bulky in size to use. A change of approach was, therefore, taken.

3.2.3. The Revised Approach.

The transformer XF indicated in figure 3.2. is broken up into four individual transformers XFi whose primary windings Wi1 (i=1, 2, 3, 4) are connected in series and placed within the series resonant circuits, governed by the transistors TRi, as shown in figure 3.4. The primary windings Wi1 will carry the common resonant current i_1. Each transformer provides the power for one output channel and each of these channels is individually controlled. One of the output channels in which the described process is implemented is indicated in figure 3.5.

The primary winding W11 drives via the respective magnetic coupling the secondary windings W12 and W13 which in turn feed a conventional rectifier- - πfilter - load system. A fourth winding W14 encloses the common magnetic flux of the three other windinds. This winding is placed within a full wave rectifier bridge, whose dc output voltage is governed by a transistor Q_{o1}.

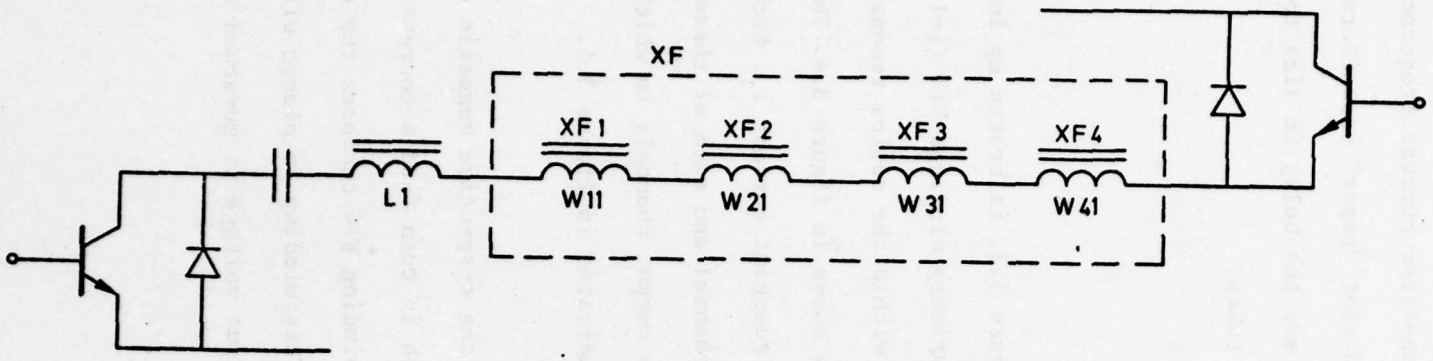

Figure 3.4. The power transformer XF, divided into four elements XFi (i=1, 2, 3, 4), placed in series within one of the resonant circuits with the thereto pertaining transistors TRi.

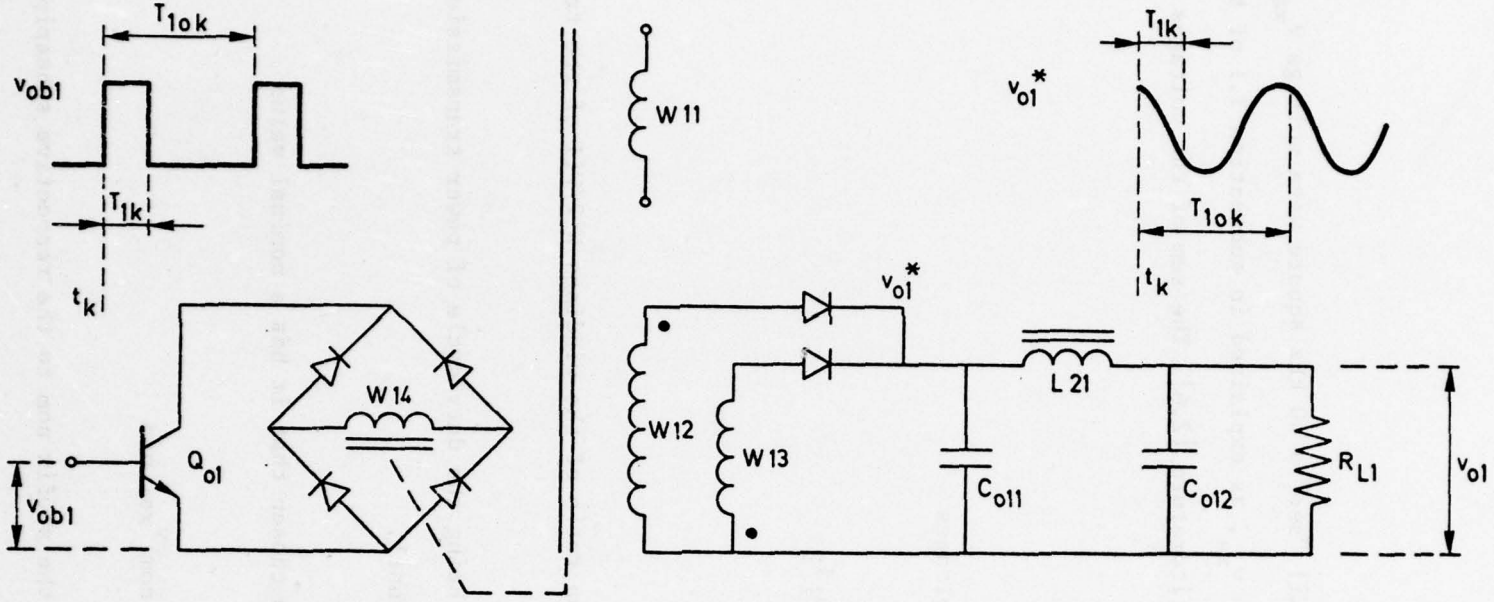

Figure 3.5. Circuit diagram of one single output channel and its power control mechanism.

The primary windings Wi1 "see" a 50 kHz square wave voltage v_{xai} with a cumulative amplitude v_{xa}, as explained in subsection 3.1 of this report and in the concerned literature [2,6]. The sum of the voltages

$$\sum_{i=1}^{4} v_{xai} = v_{xa}. \tag{3.56}$$

Each of the average voltages

$$v_{xai\ av} = v_{oi}/a_i d_i \tag{3.57}$$

where

a_i = the step up ratio of the windings Wi2/Wi1 of the transformer XFi;

$d_i = T_{ik}/T_{iok}$, being the duty cycle of power transmission in the ith output channel.

The product $a_i d_i$ is so chosen that it has a nominal value

$$a_i d_{i\ nom} \simeq v_{oi\ nom}/v_{xai\ nom} \tag{3.58}$$

which is indicated by the suffix nom to the respective subscripts. The

nominal duty cycle $d_{i\ nom}$ is so chosen that

$$d_{i\ max} - d_{i\ nom} \geq \Delta d_{i\ min} \tag{3.59}$$

where

$\Delta d_{i\ min}$ = the minimum variation of d_i from its nominal value which will guarantee that $\Delta v_{oi} < v_{oi\ max} - v_{oi\ nom}$, as specified in the Technical Guide Lines.

In lieu of a rigorous quantitative treatment of the explanation following relation (3.59), it is said here that a

$$d_{i\ max} \simeq 0{,}95\ T_{iok} \tag{3.60}$$

does, obviously, satisfy the intent of equations (3.56) and (3.57) in order to maintain the intended nominal output voltages $v_{oi\ av}$ within the prescribed tolerances. That is, if the transistors Q_{oi} are being appropriately controlled by their respective base signals v_{obi}.

The signals v_{obi} are being generated by a common control system that will be described shortly. The base signal v_{ob1} shown in figure 3.5 causes a short circuited transformer XF1, whenever transistor Q_{o1}

is energized during the shown time interval T_{1k}. The output voltage v^{*}_{o1} of the same transformer is then reduced to near zero, as implied in the same figure.

The base signals v_{obi} thus control the volt-seconds that will be "seen" by any of the individual π filters will input capacitors C_{oi1}. These base signals, when appropriately generated, thus provide individual and independent control for each of the output channels.

It is recalled at this point, that the resonant current i_1 emanates from a controlled current source. Even if all transformers XFi were to be short circuited concurrently by their resprective transistors Q_{oi}, no harm would come to transistors TRi since the currents which are carried by each of these transistors and their collector to emitter voltages would not exceed a preset limit under any confluence of adverse conditions of operation |2|.

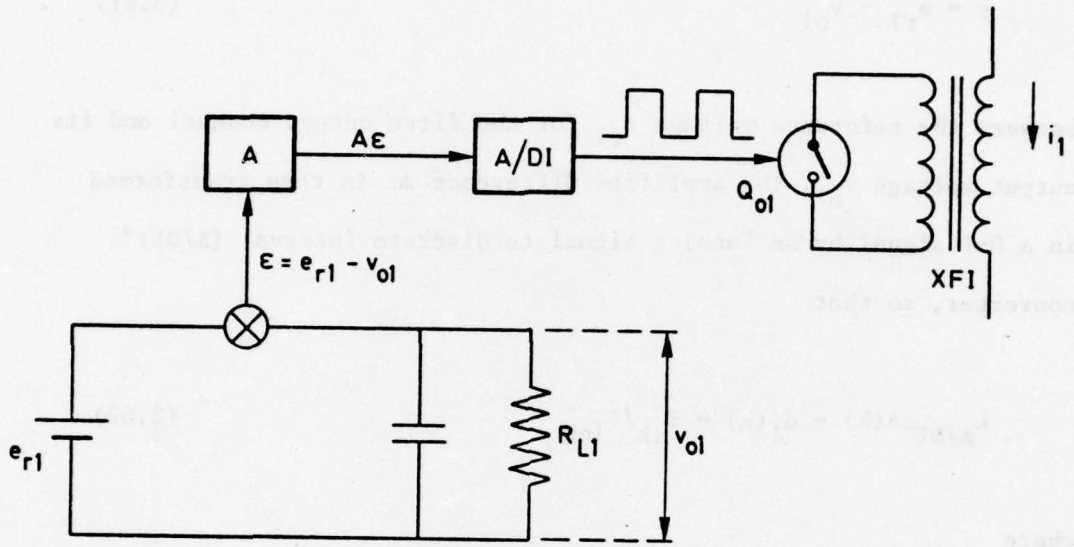

Figure 3.6.

Individual voltage control system for the first output channel.

The above referred to control system which generates the voltages v_{obi} for the output channels is indicated for channel 1 in figure 3.6. A common comparator establishes the voltage difference

$$\varepsilon = e_{r1} - v_{o1} \tag{3.61}$$

between the reference voltage e_{r1} for the first output channel and its output voltage v_{o1}. The amplified difference $A\varepsilon$ is then transformed in a 0-1 signal by an "analog signal to discrete interval (A/DI)" converter, so that

$$k_{A/DI}\varepsilon A(k) = d_1(k) = T_{1k}/T_{1ok} \tag{3.62}$$

where

$k_{A/DI}$ = a constant of proportionality;

$d_i(k)$ = the duty cycle for the kth pulse in the sequence of an infinite number of pulses.

Each of the four output channels has its own control system which is a duplicate of the one shown in figure 3.6; they control the thereto pertaining output channels which are duplicates of the one shown in figure 3.5.

3.2.4. Revised Output Filter Requirements.

One of the significant reasons to revise the approach concerning the output channels was the bulkyness of "paper" capacitors of a sufficient size to minimize the output voltage ripples for purpose of : (1) distribution of equally prorated and time invariant voltages to the output channels and (2) containment of the output voltage ripple within prescribed limits.

The π type filters in the output channels were chosen in conjunction with the described individual control mechanisms in order to accomodate the conditions, as described in the proceeding paragraph.

It would now suffice if the voltage waveforms v^{*}_{oi} that were to appear at the input capacitors C_{oi1} of the π type filters were to satisfy the requirement that

$$v_{oi\ nom}(1-\Delta i) + i_{oi}R_{L2i} < v^{*}_{oi\ av} < v_{oi\ nom}(1+\Delta i) + i_{oi}R_{L2i} \qquad (3.63)$$

where

$$\Delta_i = (v_{oi\ max} - v_{oi\ nom})/v_{oi\ nom}$$

i_{oi} = the dc current in the ith load

R_{L2i} = the resistance of the inductor in the concerned filter.

$v_{oi\ nom}$ = the average nominal voltage of the ith output channel.

The voltage ripples of the voltage v_{oi} are then mitigated by appropriate choice of the remaining part of the individual filters. One of the voltage waveforms v_{oi} is illustrated in figure 3.5, to wich general reference is made for the following discussion.

It is desirable to keep the current form factors

$$\rho_{ij} = i_{Loj\ rms}/i_{oj} \qquad (j= 1,2,3,4) \qquad (3.64)$$

as near to unity, as practically possible in order to limit the copper losses in the inductors L_{oj}. For that purpose it is first assumed that

$$v_{oi} > 0 \qquad (3.65)$$

at any time. The voltages v_{oi} of capacitors C_{oil} were defined with reference to figure 3.5.

In order that (3.65) be satisfied it is necessary that

$$\frac{2}{T_{ok}} \int_{t_k}^{t_{k+1}} |v_{c2}|\, dt > v_{c2pp} \qquad (3.66)$$

where

v_{c2} = the voltage on the fictitious capacitors C_2 defined with reference to equation (3.7), but now with a quantitative meaning as required by the newly introduced conditions (3.65) and (3.66) ;

v_{c2pp} = the peak to peak value of v_{c2}.

The value of C_2 then results from the condition that

$$i_{1\,av}\, T_{ok} = C_1 v_{c1pp} = C_2 v_{c2pp} \qquad (3.67)$$

since then two capacities C_1 and C_2 carry the same resonant current i_1. It follows that if

$$C_2 = C_1 v_{c1pp} / v_{c2pp} > C_1 v_{c1pp} / 2 v_{2av} \qquad (3.68)$$

then

$$C_2 > 10^{-6}\ 88/34 \simeq 2.6\ \mu F. \qquad (3.69)$$

This capacitor C_2 is now the cumulative equivalent of all four secondary filter input capacitors C_{oi1}, as reflected into the primary circuit.The inequality (3.69) can be easily satisfied with the use of currently available non-electrolytic capacitors.

The input terminals of the π filters "see" the rectified quasi-sinewave current $|i_1|$. For purpose of simplicity it is assumed here that $|i_2|$ is, indeed, a rectified sine wave current.

Examination of the well known Fourrier series

$$i_r = (4I_a/\pi)\{(1/3)\cos 2\omega_F t - (1/15)\cos 4\omega_F t + ...\} \qquad (3.70)$$

of a rectified sine wave in the light of the transfer function of a π filter results in the well founded argument, that it is sufficient to consider the first harmonic component; an adequate approximation for the purpose of filter design will result from this approximation.

In equation (3.68) is

i_r = the ac content of $|i_1|_i$

I_a = the amplitude of the resonant current i_{1i}

$\omega_F = \pi/T_{ok}$, the radial frequency which is impressed on the resonant circuits.

Reference is made to figure 3.5 in support of the following discussion: The transfer function which relates the output voltage ripple v_{ri} of the ith channel to the input current ripple i_{ri} to the π filter of the same channel is given by

$$v_{ri1}/i_{ri1} = \frac{R_{Li}}{(1 + R_{Li}C_{oi2}S)(1 + L_{2i}C_{oi1}S^2) + R_{Li}C_{oi1}S} \qquad (3.71)$$

where

i_{ri1} = the first harmonic component of i_{ri}

v_{ri1} = the first harmonic component of v_{ri}.

It is anticipated that :

$$R_{Li}C_{oi1}2\omega_F >> 1$$
$$R_{Li}C_{oi2}2\omega_F >> 1 \qquad (3.72)$$
$$L_{oi}C_{oi1}4\omega_F{}^2 >> 1$$

and

$$L_{oi}C_{oi1}4\omega_F{}^2 >> R_{oi}C_{oi1}2\omega_F$$

The attenuation a_{F1} of the first harmonic component of the series (3.70), is then approximated by :

$$a_{F1} = \left|\frac{i_{ri1}R_{Li}/|i_{2i}|_{av}}{v_{ri1}/V_{oi}}\right| \simeq (2R_{Li}C_{oi2}\omega_F)(4L_{oi}C_{oi1}\omega_F{}^2)\ V_{oi}/|i_{2i}|_{av} \qquad (3.73)$$

Each of the harmonics was normalized with respect to the average values of v_{oi} and $|i_{2i}|$, respectively

$$a_{F1} \simeq 8R_{Li}C_{oi1}C_{oi2}L_{oi}\omega_F{}^3\ V_{oi}/|i_{2i}|_{av} \qquad (3.74)$$

Examination of (3.70) and (3.74) indicates that

$$a_{F2} \simeq 64 R_{Li} C_{oi1} C_{oi2} L_{oi} \omega_F^3 V_{oi} / |i_{2i}|_{av} \qquad (3.75)$$

for the second harmonic component that would amount to only 1/5 of the magnitude of the first. In short the second harmonic component would have at the filter's output terminals only 1/(8)(5) = 1/40 of the magnitude of the first. The contribution of the second harmonic to the over all output voltage ripple is then approximated by

$$v_{ri} \simeq v_{r1}\{1 + (1/40)^2\}^{\frac{1}{2}} \simeq v_{r1}(1.012). \qquad (3.76)$$

The error caused by omission of the higher harmonic components of (3.70) is of the order of one percent, and is well within the tolerances of the concerned filter components.

Relations (3.68) and (3.74) provide sufficient information for the design of the individual output filters in order to meet the requirements of the above referred to Technical Guidelines.

The concerned capacitors for the $\pm$ 15 V and $\pm$ 5 V channels will divide according to the respectively processed power.

Thus

$$C_{2-12} = C_2\ 100/190 \simeq 0{,}5\ C_2 \qquad (3.77)$$

and

$$C_{2-34} = C_2\ 90/190 \simeq 0{,}5\ C_2 \qquad (3.78)$$

where

C_{2-12} = that part of C_2 which is reflected by the 5V channels with a nominal power of 2 x 5 x 10 Watts;

C_{2-34} = is the analogous part for the 15 V channels.

A simple active damping circuit is used to limit overshoots of the output voltages v_{oi} during the turn-on phase and during related dynamic conditions.The output terminal is then temporarily clamped to ground via an oversize load resistor R_z. This clamping function is implemented by a transistor Q_z, whose base in turn is energized from the output terminal via a Zemer diode D_z. The diode D_z has the appropriate Zemer voltage , so that Q_z would not be energized when $v_{oi} < v_{oi\ nom}\ (1+\Delta)$, but when this voltage is exeeded by a margin of, approximataly, 5 percent.

3.3. Identification of Critical Aspects

3.3.1 Functional Requirements

Operation of the converter in its full bridge configuration requires ascertainment that both transistors which conduct the resonant current simultanously be "turned off" before turning on the companion pair of transistors.

The "turn off" process is implemented by clearing of the transistor junctions whereby the charge which remains in the junction after termination of the resonant current is removed. A negative, low impedance base signal is applied for that purpose. Currents up to 1 A appear for short time intervals, depending on the characteristics of the power transistors. Removal of a charge of approximately 0.5 µC within 0.5 µsec. is not uncommon and may yet increase at higher temperatures.

Signals, which comfirm that the junctions of the transistors which have been carrying current are cleared, are used to open the gates which otherwise prevent the "firing" of the companion transistor pair. The just named signals now replace the formerly used signals which announce the state of back bias of the power thyristors. It was found that this state of back bias does not "guarantee" that a transitor has been turned off, since it can be conducting in the reverse direction, unlike the thyristor for which the turn off condition is assumed after a given number

of microseconds following its back bias condition.

Completion of the process of extraction of charge from the formerly conducting transistor is presumed when its base voltage falls from the minimum forward voltage drop during conduction of approximately 600 mV to a negative value which is then limited for purpose of protection of the base-emitter junction.

Small size high frequency (MHz) pulse transformers were used for that purpose. The received signal is then used to change the state of one bistable circuit which in turn governs the access to the firing circuits of the two transistor pairs, blocking one part and leaving the other open.

3.3.2 Streamlining of the Protection System for 50 kHz Operation

The eletronic system which prevents simultanous firing of transistors which do not belong to the same pair, used in the previous phase of the program was a converted thyristor protection system. It is based on the philosophy that a thyristor should not be fired unless its companion has (1) ceased to conduct and (2) enough time has

passed to presume that its junction is cleared. As explained above, it is possible to establish clearance of a transistor junction by observing the base to emitter voltage v_{be} and deriving an appropriate signal therefrom. No further delay is needed, and the companion transistor can be fired immediately thereafter.

The just explained difference in the characteristics of transistors and thyristors allows application of a different protection philosophy, which greatly simplifies the concerned electronics.

One single bistable circuit is now used which is triggered in succession by the signals which emanate from the change of polarity of the base-emitter junction in the negative direction. The signal which initiates the junction clearing must preceed the junction clearing signal; it is derived from the change of polarity of the resonant current at the end of the resonant half cycle. This signal is used to terminate the proportional base drive of the power transistor and to initiate simultanously the junction clearing process; no change of state of the bistable circuit is caused by the just described base drive termination and junction clearing process.

The new process of protection and control, described in subsection 3.2.3, can be briefly summarized as follows:

a. termination of one half resonant current cycle is detected and a signal to that effect generated;
b. the signal identified under a. terminates the current pulse through the respective transistor by (1) removing the base drive and (2) engaging the junction clearing mechanism;
c. completed clearence of the power transistor junction is signaled to the governing bistable electronic mechanism which changes state and thus clears the way for the request of the control mechanism for the next current pulse.

3.3.3 The Magnetic Components at 50 kHz.

The magnetic components hold one of the keys for the access to the 50 kHz range. Study of the concerned magnetic core materials pointed the way to the low loss 3H1 type ferrite. This material can be used for maximum flux densities up to 0.2 Tesla, leaving a reasonable margin to its maximum flux density near 0,3 Tesla.

The 3H1 material appears not to be currently used for power applications and is, therefore, not available in th form of conventional power core configurations. Use had to be made of, so called "cup cores", often found in communication technology.

During progress of the development phase it became obvious that the application of Litz-wire as magnet wire would be almost mandatory. The urgency to complete the program would not allow the rather long lead time of more than one year to acquire Litz wire. Stranded wire consisting of fine individual strands of wire was, therefore, used instead; this entailed the therewith associated added power losses in the magnetic devices.

The concerned magnetic devices, the series inductors, the power transformers and the output inductors, yielded nevertheless acceptable qualities to complete the program.

3.3.4. Cooling

Cooling by convection was applied. A total heat load of a maximum of 45 Watt requires careful design of the magnetic components and

appropriate mounting of the semiconductor components which will generate most of the heat.

4. Design and Development.

4.1. General Aspects.

The presented circuit design study is based on the assumption of a frequency of inversion of 50 kHz. The technical goal of a power density of 50 W/kg may have been attainable with a lower internal frequency of converter operation. It appeared, however, appropriate to demonstrate the feasibility of transistor operation at the higher frequency. The power density of components is estimated at 158 W/kg, well in excess of the goal as defined in the Revised Technical Guidelines for work under this contract.

The designed circuit, as presented here, differs from the previously built 100 Watt model in that a full bridge configuration is used, instead of the former half bridge configuration. A larger current capacity is brought into the realm of the transistorized series inverter-converter by use of the full bridge configuration. The usefulness of transistors has been extended through the work under the current program: a method was found that limits current peaks unconditionally, even under start-up or other transient conditions of operation. Derating of transistors should not be necessary because of the well known phenomenon of unexpectedly high current spikes.

The individual power losses in the circuit components, their projected weight and the efficiency of the system are listed in the following.

Tabulation of Estimated Physical Weights and Power Losses of the Components for the 190 Watt Breadboard.

Component		Power Loss Watts	Weight kg.
Power Circuit:			
Input Filter Capacitor	C_i		.050
Series Capacitor	C_1		.020
Transformers	XF	4.000	.175
Series Inductor	L_1	2.100	.180
Transistors and Diodes	TRi, Dij	18.000	.140
Output Rectifiers	D2ij	18.000	.100
Output Capacitors	C_{oij}		.200
Output Inductors	L_{oi}	2.000	.180
Miscellaneous Losses		4.235	.155
Subtotals		50.000	1.200
Control System Components		4.000	.300
Total		54.000	1.500

Estimated Efficiency: 77.86 %

Estimated Power Density: Components: 126 W/kg; Packaged (160%): 80 W/kg.

4.2. System Design.

The system is to operate from a dc source with a nominal voltage $E_s = 28$ V. The tolerated variations of the input voltage, as defined in the Revised Technical Guidelines of 19 November 1974 are contained in the statement

$$E_{s\,min} = 22 < E_s < 32 = E_{s\,max} \qquad (4.1)$$

The input voltage variation indicated in (4.1) is relativly moderate, compared to the capability of the series capacitor inverter-converter to accomodate these variations. Input voltage ratios $E_{s\,max}/E_{s\,min} = 2$ are not uncommon for this type of converter. This relativly wide range of input voltage variations is facilitated by the converter's intrinsic property to maintain a relativly constant current form factor i_{1rms}/i_{1av} for appreciable variations of the input voltage, which in turn causes little change in the dissipation losses of the system for a given average current level.

The full bridge configuration of the primary circuit of the converter comprising a series resonant circuit is shown in figure 4.1. The shown configuration was chosen to limit the transistor currents to magnitudes which could be easily attained with currently available components.

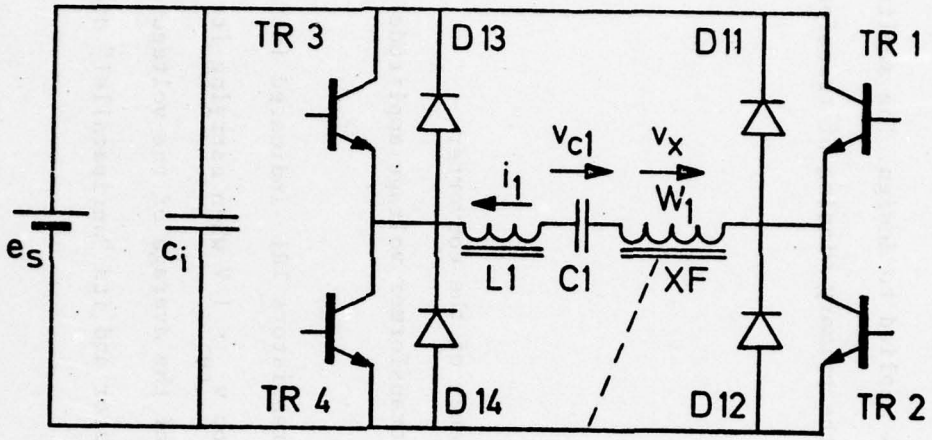

Figure 4.1.

Primary circuit of the series resonant circuit converter.

Analysis of currents and voltages in full bridge series inverters which is closely related to the analysis for half bridge converters and partially treated in subsection 3.1, is now applied to design. The amplitude v_{xa} of the "square wave" voltage v_x on the primary winding of transformer XF is here

$$v_{xa} = qe_s \simeq \eta e_s \qquad (4.2)$$

where

η = the estimated efficiency of the converter

$q = v_{xa}/e_s$ the ratio of transformer voltage amplitude and source voltage e_s.

Assumed is that each of the transistors TRi indicated in figure 4.1 will develop an average voltage drop $v_{ce} < 1$ V when carrying its maximum current. Or more exactly: the maximum of the average of the voltage drops which develop in succession over the transistor and its "antiparallel" diode Dij is assumed to be 1 Volt.

The net available minimum dc voltage $e_{s\ min}$ that is impressed on the resonant circuit is then

$$e_{s\ min} = 22 - 2 = 20\ V \qquad (4.3)$$

For $\eta = .75$ as assumed on the outset of this work is

$$v_{xa} \simeq (0.75)(22) \simeq 17 \text{ V} \tag{4.4}$$

Relation (4.4) indicates the net voltage on the primary winding of the transformer as viewed from the load.

The average current

$$i_{l\ av} = 190/17 = 11.18\ A_{av}; \tag{4.5}$$

its estimated rms value at full load

$$i_{l\ rms} = (1.3)(11.18) \simeq 14.5\ A_{rms} \tag{4.6}$$

The steady state current peak value at full load is approximated by

$$I_l \simeq (11.18)(\pi/2) \simeq 18\ A_p \tag{4.7}$$

The capacitor voltage v_{cl} will rise to a value in excess of

$$v_{cl\ max} > E_s + v_{xa}/q + 2v_{ce} + e_n \tag{4.8}$$

where

e_n = the net driving voltage of the series resonant circuit.

The value for e_n is, conveniently, referred to the steady state operation of the system as stated in (4.2) so that

$$e_n = E_s(1 - q) \simeq 5 \text{ V} \tag{4.9}$$

The peak to peak voltage v_{c1pp} of capacitor C_1 is calculated from (4.8) to be

$$v_{c1pp} = 2v_{c1\ max} \simeq 2(22 + 22 + 2 + 5) = 102 \text{ V} \tag{4.10}$$

for $e_s = e_{s\ min} = 20$ V and $i_{1\ av} = i_{1\ av\ max} = 11.2$ A.

The value of capacitor C_1 is now reviewed, using the relation

$$C_1 = \frac{i_{1\ av\ max}\ T_{ok\ min}}{v_{c1pp}} \tag{4.11}$$

or

$$C_1 = (11.2)(10.10^{-6})/94 \simeq 1\mu\text{F} \tag{4.12}$$

The value of inductor L_1 follows from

$$L_1 = (T_o/\pi)^2/C_1 \qquad T_o = 9\ 10^{-6}\ \text{sec.} \tag{4.13}$$

and yields

$$L_1 \simeq 8.5\ \mu H \tag{4.14}$$

The distributed inductance in the circuit and the leakage inductance of the transformer XF should suffice to provide one part of the inductance given by relation (4.14).

Four output channels are planned for the secondary circuit. Two for output voltages

$$v_{o1} = |v_{o2}| = 5\ V \tag{4.15}$$

and with an average current

$$i_{21\ av} = i_{22\ av} = 10\ A \tag{4.16}$$

Two other channels provide output voltages

$$v_{o3} = |v_{o4}| = 15 \text{ V} \tag{4.17}$$

with average currents of

$$i_{23\ av} = i_{24\ av} = 3 \text{ A} \tag{4.18}$$

as required in the Technical Guidelines for Advanced Power Processing Techniques (TGA).

The output voltage peak to peak ripple v_{rpp} is limited by the TGA to

$$100\ v_{rppi}/V_{oi} \leq 0.05; \quad i = 1, 2, 3, 4 \tag{4.19}$$

where

$V_{oi} = \frac{1}{2}(v_{oi\ min} + v_{oi\ max})$, the nominal voltage of the ith output channel.

An equivalent capacitor C_2 is first assumed to be the filter capacitor for one single output channel for the total power

$$P_o = (2)(50)+(2)(45) = 190 \text{ W} \tag{4.20}$$

at an arbitrary voltage of 17 V. The equivalent output current

$$i_2 = i_1 \tag{4.21}$$

under these conditions. The largest output voltage ripple occurs under conditions of lightest loading and the highest input voltage $e_{s\ max}$. The maximum variation Δv_o of the output voltage then occurs between inception and termination of one current pulse. The average current

$$|i_2|_{av\ c} = |i_1|_{av\ max} e_{s\ max}/e_{s\ min}/\rho_{vi} \tag{4.22}$$

where

$|i_2|_{av\ c}$ = the value of the average current i_2 as defined before for $e_s = e_{s\ max}$ when $T_{ok} = 2T_o = 2\pi\sqrt{L_1 C_1} = 2\pi/\omega_o$.

$$\rho_{vi} = (e_{s\ max}/e_{s\ min})\ (|i_1|_{av\ max}/|i_1|_{av\ min}) \tag{4.23}$$

The "firing angle" ψ_r is a function of ρ_{vi} as discussed with reference to figure 7 in reference 6. reproduced here for convenience as figure 4.2.

The ratio

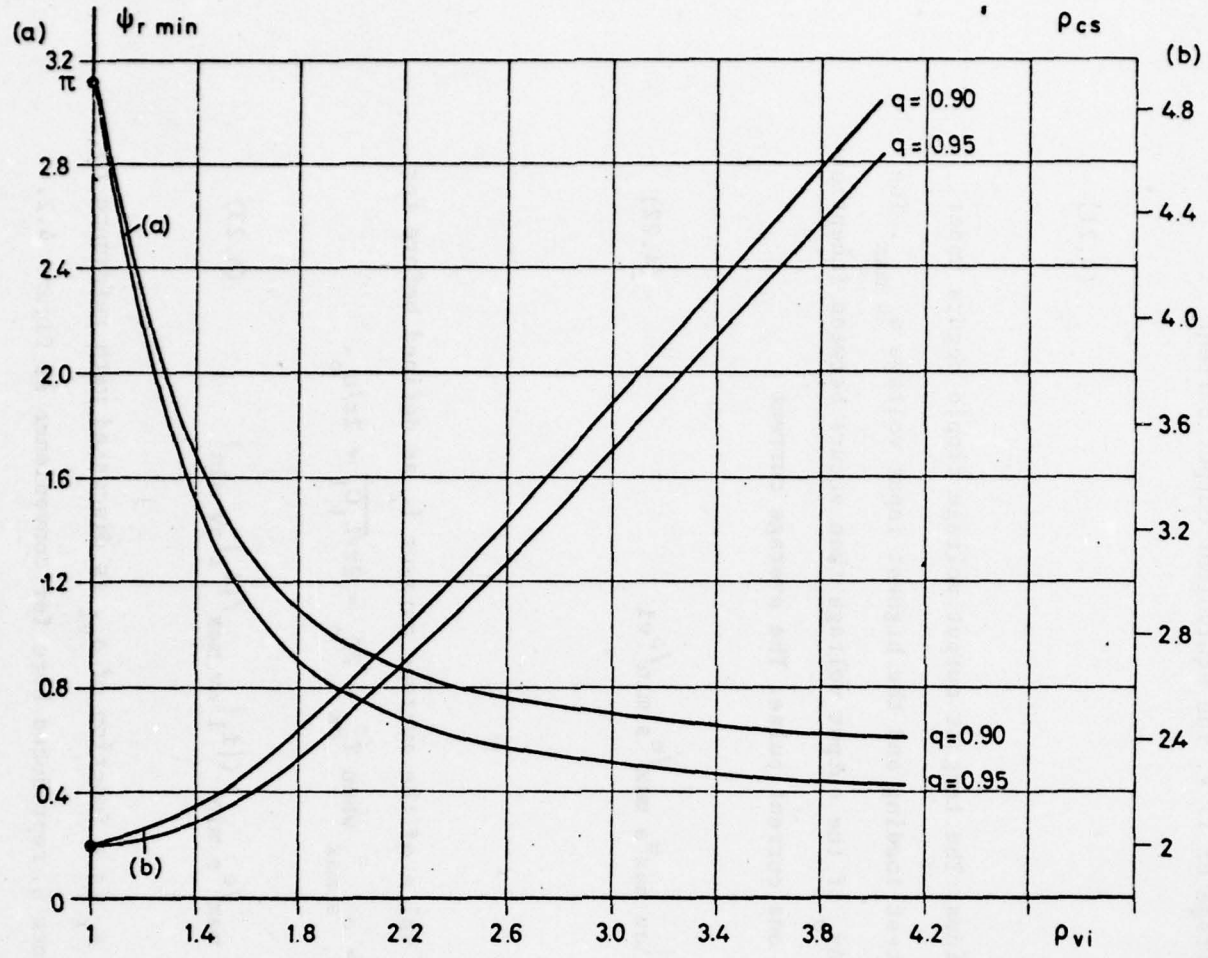

Figure 4.2.

(a) Minimum angle $\psi_{r\ min}$ as function of $\rho_{vi} = (e_{s\ max}/e_{s\ min})(|i_1|_{av\ max}/|i_1|_{av\ min})$; calculated from

$$\psi_{r\ min} = \arccos \frac{1 - (1 + \gamma)\rho_{vi}\ q/(1 + q)}{1 - (1 + \gamma)\rho_{vi}/1 + q)} \quad ; \quad q = 2v_{xa}/e_{s\ min}$$ (see figure 2); $\gamma = (\psi_r - \psi_o)/\pi$

(b) ratio $\rho_{cs} = v_{cpp\ max}/e_{s\ max} = (1 + \gamma)(|i_1|_{av\ max}/|i_1|_{av\ min})$.

$$e_{s\ max}/e_{s\ min} = (32-2)/(22-2) = 1.5 \qquad (4.24)$$

The minimum "firing angle" $\psi_{r\ min}$ is assumed to be 0.25 π. Extrapolation for q = 0.75 in said figure 7 shows that a $\rho_{vi} \simeq 6.0$ can be attained when ψ_r varies from 0.25 Π to π. Rearrangement of (4.23) yields

$$|i_1|_{av\ min} = |i_1|_{av\ max}\ e_{s\ max}/e_{s\ min}/\rho_{vi} \qquad (4.25)$$

and combination with (4.5) and (4.25) yields that

$$|i_1|_{av\ min} = (11.2)(1.5)/6 \simeq 2.8\ A \qquad (4.26)$$

whereby

$$|i_1|_{av\ min} = |i_2|_{av\ c} \qquad (4.27)$$

as defined under (4.22).

The average value of $|i_2|_{av\ c}$ cannot be altered by any lower current demand because the pulses will then become separated, but unchanged in shape and content.

The largest variation Δv_o of the assumed output voltage v_o occurs when

$$\Delta v_o = (1/C_2)|i_2|_{av}\, c T_{ok\ max} \qquad (4.28)$$

where

$T_{ok\ max} = 2T_o$ as explained in the literature |2|.

The conditions which govern the individual output filters are now analyzed to determine the needed attenuations.

The average secondary current $|i_{21}|_{av}$ which enters the first 5 V output filter

$$|i_{21}|_{av} = i_{o2} = 10\ A; \qquad (4.29)$$

this is in accordance with the TGA. The ripple content i_{r1} of the first harmonic component of this current is given by

$$i_{r1} = (2/3)|i_{21}|_{av} \cos 2\omega_F t \qquad (4.29)$$

since

$$I_{a21} = (\pi/2)|i_{21}|_{av} \qquad (4.31)$$

where

I_{a21} = the amplitude of the resonant current i_{21} which enters the rectifier of the first output channel;

$\omega_F = \pi/T_{ok\ av}$, being the radial frequency of the resonant current.

The peak to peak ripple i_{r1pp}, normalized with respect to $|i_{21}|$ is derived from (4.30) by writing

$$i_{r1pp}/|i_{21}|_{av} = (4/3) \cos 0.628\ 10^6 t \qquad (4.32)$$

The TGA limits the normalized peak to peak output voltage ripple v_{ripp}/v_{oi} to $\pm$ .0005, as stated in (4.19). The attenuation a_{F11} which has to be performed by the filter of the +5 Volt channel is given by

$$(i_{r1pp}/|i_{21}|_{av})/(v_{r1pp}/V_{o1}) = a_{F11} \qquad (4.33)$$

The numerical values, given in (4.21) and in the TGA are introduced in (4.33) to yield

$$a_{F11} = (4/3)/0.005 \simeq 267 \qquad (4.34)$$

Use is now being made of the approximation (3.74)

$$267 \simeq (8)(0.5)C_{o11}C_{o12}L_{o1}(0.628\ 10^{6})^{3}(5/10) \qquad (4.35)$$

yielding that

$$C_{o11}C_{o12}L_{o1} \simeq 538\ 10^{-18} \qquad (4.36)$$

The break down of the product on the left hand side of (4.36) is in this case, primarily, governed by practical considerations, limited by the inequality (3.68) and the therefrom derived minimum value of $C_2 > 2.6\ \mu F$, as stated in (3.69).

From (3.77) it is derived that

$$C_{o11} > \tfrac{1}{2}(17/5.5)^{2}(0.5)(2.6)10^{-6} \simeq 6.2\ \mu F \qquad (4.37)$$

The factor $\frac{1}{2}$ stems from the fact that one of the 5 Volt channels is being considered; the factor $(17/5.5)^2$ is needed for the transformation of the respective impedance levels,

The capacitor C_{o11} has to accomodate a current ripple with an rms content of

$$i_{r1\ rms} \simeq (2/3)(10/\sqrt{2}) \simeq 4.68\ A_{rms} \qquad (4.38)$$

at the 100 kHz fundamental frequency. Smaller siza "paper" capacitors are, usually, limited to rms currents of 0.25 to 0.5 A_{rms}. A value of

$$C_{o11} = C_{o21} = 20\ \mu F \tag{4.39}$$

was applied for the intended purpose.

The capacitors

$$C_{o12} = C_{o22} = 20\ \mu F \tag{4.40}$$

were dimensioned as indicated in (4.40) for the purpose of simplicity of construction. The value of the filter inductor had to conform to

$$L_{o1} > (5375/(20)(20)(10^{-12}))\ 10^{-18} \simeq 13.5\ \mu H \tag{4.41}$$

A generous margin of an order of magnitude is allowed in relation (4.41) to accomodate the parasitic inductive and resistive elements of the capacitors. Another factor of more than two is allowed for the above referred to loading conditions. Thus

$$L_{o1} \simeq 36\ \mu H \tag{4.42}$$

was chosen for that purpose. The same filter component values apply for the -5 Volt channel.

By an analogous process of reasoning it was established that $C_{o31} = C_{o41} = 10\ \mu F$, and that $C_{o32} = C_{o42} = 50\ \mu F$. The inductors

$$L_{o3} = L_{o4} = 32\ \mu H. \tag{4.43}$$

Design of the magnetic components is treated in subesection 4.3.2.

A maximum input voltage ripple has not been specified, since this system could be powered from a battery source of electric energy, The size of the input filter capacitor C_i is, therefore, only estimated to be determined by

$$C_i > \tfrac{1}{2}\, i_{l\ av\ max}\, T_{ok\ min}/e_{ipp} \tag{4.44}$$

where

e_{ipp} = the peak to peak variation of the converter input voltage if capacitor C_i were the only energy storage facility in a current source i_s.

A ratio

$$e_{ipp}/e_{s\ nom} = .05 \tag{4.45}$$

is chosen arbitrarily for purpose of design. The input capacitor

$$C_i > (5.8)(10^{-5})/(1.4) \simeq 40\ \mu F. \qquad (4.46)$$

4.3. Critical Components.

4.3.1. Semiconductor Components.

Transistors of the type 2N5330 have been selected for construction of the system. These transistors will perform the functions of the transistors TRi identified in figure 2.4. They can carry a maximum direct current of 30 Amperes, which is well below the peak value $I_1 = 18\ A_p$ given in relation (4.7). A new anticipating type current peak predicting and limiting technique will be incorporated in the control system, thus limiting the absolute maximum instantanuous value of the current unconditionally to a maximum such as 22 Amperes. The just described new control feature should greatly enhance the reliability of the system as a whole, being a safeguard against one of the most common causes of transistor failure: the occurrance of sudden current peaks due to the confluence of adverse transient operating conditions.

Containment of the peak current I_1 appears as the most important feature to secure safe transistors operation. The other significant limiting characteristics such as the average current

$$\tfrac{1}{2} i_{1\ av\ max} = 5.8\ A << 30\ A_{rated} \qquad (4.47)$$

The same holds for the maximum collector to emitter voltage

$$v_{ce\ max} = 33\ V << 100\ V_{rated} \tag{4.48}$$

The maximum cumulative power dissipation P_{dc1} caused by current conduction in all transistor-diode pair combinations is estimated at approximately

$$P_{dc1} = (0.6)(11.2)(2) = 13.5\ Watt \tag{4.49}$$

where $v_{ce\ av} = 0.6$ V for $i_{1\ av} = i_{1\ av\ max}$, based on the previous experience with transistor series capacitor inverter-converters as documented in the Interim Report prepared under this contract.

Added is the power loss in the base-emitter circuits which consist of the power loss P_b caused by the base drive signal

$$P_b = (2)(2)f_i(T_k/T_{ok}) \int_0^{T_k} v_{be} i_b \, dt \tag{4.50}$$

where

f_i = frequency of inversion;

T_k/T_{ok} = duty cycle of transistor current conduction for full power operation;

v_{be} = base to emitter voltage;

i_b = base current.

Factors (2) in (4.50) refer to the number of (a) simultanuously conducting transistors and (b) switching events per cycle of the inversion process. The power lost in the base circuit

$$P_b = (2)(2)(0.8)(50\ 10^3)(0.8)(8\ 10^{-6})(18/10)(2/\pi) \simeq 1.2\ W \quad (4.51)$$

The power loss in the switching elements of the primary power circuit P_{dsl} due to switching operation is estimated to 300 mW, based on previous experience on the 100 Watt model.

The total power loss P_{dl} of the switching components in the primary circuit is estimated

$$P_{dl} = P_{dcl} + P_{dsl} + P_b \simeq 15\ Watt \quad (4.52)$$

The above referred to "antiparallel" diodes Dli are of the type SVD50-12. These diodes can easily handle the maximum average currents

$$i_{Dl\ av\ max} < (1/10)(11.2) = 1.12\ A \quad (4.53)$$

Both, the selected transistors and the thereto pertaining diodes have

fast switching characteristics (less than 100 nanoseconds) which proved favorable in the preceding study. The dissipation losses of the diodes Dli are included in (4.49).

Ultra fast switching Schottky barrier diodes TRW SD41 were chosen as diodes D2ij (i,j = 1,2) for the 5 Volt output channels, indicated in fidure 2.2. The forward voltage drop v_{F2i} in these diodes is estimated to be

$$v_{F2S} \simeq 0.5 \text{ V at } i_F = 10 \text{ A} \tag{4.54}$$

The power loss in these diodes due to current conduction P_{d2cS} is estimated to be

$$P_{d2cS} = (2)(0.5)(10) = 10 \text{ Watt} \tag{4.55}$$

The reverse current i_{rev} in each of these diodes at 10 V back bias and approximately 70 ^{o}C junction temperature is estimated at 30 ma. The therefrom resulting power loss

$$P_{d2rS} = (2)(10)(0.03) = 0.6 \text{ Watt} \tag{4.56}$$

Switching losses in Schottky barrier diodes appear to be a minor loss component. The maximum total power loss P_{d2S} in the switching elements

of the two 5 V output channels is therefore estimated

$$P_{d2S} \simeq 11 \text{ Watt} \tag{4.57}$$

The maximum losses in the diodes TRW, SVD50-12 in the 15 V channels are estimated

$$P_{d2cS} = (2)(1)(3) = 6 \text{ Watt} \tag{4.58}$$

The switching losses in these diodes

$$P_{d2sS} \simeq 1.26 \text{ Watt} \tag{4.59}$$

A total loss of

$$P_{d2J} = 7.26 \tag{4.60}$$

in the switching components of the 15 V channels is therefore anticipated. The total switching loss P_{d2} in all output channels is, therefore, estimated to

$$P_{d2} = 10.6 + 7.26 \simeq 18 \text{ Watt} \tag{4.61}$$

The switching losses of all semiconductor components of the power system

$$P_d = P_{d1} + P_{d2} \simeq 15 + 18 = 33 \text{ Watt} \tag{4.62}$$

4.3.2. Magnetic Components.

The four power transformers XF_i (i = 1,2,3,4) were identified with reference to figure 3.4. The primary windings W_{i1} of these four transformers carry the same resonant current i_1. The voltages v_{xai} which appear on each of these primary windings W_{i1} divide according to the power which they transfer to the secondary circuits. Thus

$$v_{ax1} = v_{ax2} = 17(50/190) \simeq 4.47 \tag{4.63}$$

and

$$v_{ax3} = v_{ax4} = 17/(45/190) \simeq 4.03 \tag{4.64}$$

Each of these transformers XF_1 and XF_2 has to transfer, approximately, 55 Watt of power to feed a 0.5 Ohm load with 10 Amperes via Schottky barrier diodes with a voltage drop of nearly 0.5 Volt. It was, arbitrarily, assumed that each of these transformers would have a loss of 1 Watt. This 2 percent power loss was a ompromise to arrive at a favorable efficiency

with the intended advantage of a low physical weight.

The cup core of 3H1 ferrite material P/30/19 was chosen for construction of all four transformers XF_i as indicated in figure 3.4. This core material has a power dissipation of approximately 50 mW/cm^3 at a frequency of 50 kHz and a maximum flux density of 0.2 Tesla. The core has a net weight of 34 g. The primary windings W_{i1} are implementd by strands of 13 individually enameld copper wires with a diameter of 0.4 mm

The 5 V transformers have primary windings W_{i1} with four turns each. The secondary windings of the same transformers consist of 5 turns, composed of ten wires with diameters of 0.4 mm. The control windings W_{14} and W_{24} consist of 40 turns; one single copper wire of 0.4 mm diameter is used for that purpose. The total weight of each of these transformers is, approximately 45 g.

The 15 V transformers are similarily constructed, except that only three turns are used for the primary windings W_{31} and W_{41}, respectivly. This is consistent with relations (4.63) amd (4.64). The secondary power windings have a larger number of turns, namely 12, consisting of four wires with diameters of 0.4 mm, each. The control windings W_{34} and W_{44} have 30 turns each, again, consisting of one single wire of 0.4 mm diameter. The weight is the same as that for the 5 V transformers.

The actual weight of all four transformers was established as

$$W_{TXF} \simeq 180 \text{ g} \tag{4.65}$$

with a cumulative calculated power loss of

$$P_{Loss\ XF} \simeq 4 \text{ Watt} \tag{4.66}$$

A cup core of the same type ferrite material 3H1 was used to control the series inductor. A somewhat larger core P/42/29 was used for that purpose. Four turns of stranded wire with a cumulative cross section of 6 mm^2 were wound around the core. An inductance of 6.2 μH was attained when an air-gap of 2 x 0.25 mm was inserted between the cup core halves. A smaller inductor with an inductance of, approximately, 1 μH was placed in series with the above described 6.2 μH inductor. This device is also constructed with the use of a P/30/19 cup core of 3H1 type ferrite material; the design follows the above indicated proceedure, using the same type of wire. The total weight of the inductors was established to be

$$W_{TL1} \simeq 175 \text{ g;} \tag{4.67}$$

the total power loss in these inductors is estimated at

$$P_{Loss\ L1} \simeq 2.1 \text{ Watt} \tag{4.68}$$

AD-A058 506 POWER ELECTRONICS ASSOCIATES INC FAIRVIEW PARK OH F/G 9/5
ADVANCED POWER PROCESSING TECHNIQUES FOR DC TO DC CONVERTERS.(U)
AUG 78 F C SCHWARZ DAAB07-74-C-0568
UNCLASSIFIED DELET-74-0568-F NL

2 OF 2
AD
A058506

END
DATE
FILMED
11-78
DDC

The four filter inductors L_{oi} which were identified with reference to figure 3.5 were constructed with the use of cup cores P/22/13 of type 3H1 ferrite material. Each of the cores weighs 12 grams. Ten turns of four parallel wires with a diameter of 0.5 mm were wound around the core, with a total cross section of 0.8 mm^2. The total weight of each inductor is 45 g. These cores were then provided with the appropriate air gaps to assume the inductances as required by (4.42) and (4.43). Each inductor has a power loss of, approximately, 0.5 Watt in each output channel. The total weight of all four inductors

$$W_{TLo} = 180 \text{ g.} \tag{4.69}$$

4.3.3. Capacitors.

The series capacitor C_1 of 1 μF will be an extended aluminum foil capacitor with polypropylene dielectric separators. This type of capacitors is produced with dissipation factors as low as 0.02 percent. The power loss in this capacitor is estimated

$$P_{CS} \approx (14.5)(1.12)(100)(2\ 10^{-4}) = 324 \text{ mW} \tag{4.70}$$

The capacitor has an estimated weight of

$$W_{CS} = 20 \text{ g} \tag{4.71}$$

The capacitor weight is relativly low, since the moderate peak capacitor voltage does not require oil impregnation.

The input filter capacitor C_i of 50 μF consists of five "paper" type 10 μF units. A dissipation factor of 0.1 percent is assumed for this type of capacitors. The power loss P_{Ci} is estimated

$$P_{Ci} = \tfrac{1}{2}\,(14{,}5)(1.12)(o.5)\ 10^{-3} = 4.06 \text{ mW} \tag{4.72}$$

The estimated weight of this capacitor is

$$W_{Ci} = 200 \text{ g} \tag{4.73}$$

The output filter capacitors C_{oij} are composed of 10 μF units of the same type as C_i. The power loss per unit is estimated at

$$P_{COl} \simeq (0.211)(5/\sqrt{2})(8\ 10^{-3}/\sqrt{2})\ 10^{-2} = 4.22\ 10^{-5} \text{ Watt} \tag{4.74}$$

$$W_{co}/\text{unit} = 10 \text{ g.} \tag{4.75}$$

The same capacitor units as the ones described above are used for all four

output channels. The total weight of all input and output filter capacitors is obtained from

$$W_{TCo} \simeq 2 \times (1 + 5 + 2 + 2) \times 16 + 5 \times 10 = 250 \text{ g.} \qquad (4.76)$$

(15 V) (5 V) (C_i)

4.4. Electronic Control.

4.4.1. The Protection System.

Protection against simultanuous "firing" of two transistors which are in immediate series connection in one leg of the full bridge configuration shown in figure 2.1 must be prevented. The termination of current flow in one pair of transistors which conduct during one half cycle is ascertained before the companion pair is "fired". The signal which indicates the above referred to termination of current conduction is the back bias voltage v_{be} of the base to emitter potential, rather than the back bias of the collector to emitter voltage v_{ce} used in the first phase of this work. Falling of v_{be} below zero is an unequivocal indication that the respective transistor junction has been cleared as a result of forced extraction of charge. Application of the just described protection philosophy has led to a substantial simplification of the concerned electronics, thus avoiding the back bias detection and signal delay process used for thyristor converters. The back bias condition of v_{be} is detected and transmitted as a 0-1 signal by suited pulse transformers for each power transistor. Appropriate logic requires simultanuous presence of these signals from

both power transistors which terminate current conduction, before the "firing" signals to the companion pair of power transistors are released. This is described with reference to figure 2.5.

Clearing of the junction of a TRW100-30 power transistor requires approximately 650 nanoseconds. Reduction of the cumulative delaying effect of all signal processing operations including clearing of the transistor junction as described above to less than 2 microseconds is requisite to attainment of a 50 kHz inversion frequency. Simplification of the protection system and elimination of a number of formerly required steps in signal processing were necessary to attain the needed "turn around" time to less than 2 microseconds. The two "memory" circuits of the former system were consolidated into one single one. The need for many otherwise required interlocking cross couplings was thus avoided. The number of needed circuit components was,accordingly, substantially reduced to less than one half of the formerly needed number.

All signal level magnetics had to be thoroughly redesigned and developed to remove delays, previously caused by leakage inductances. Transient magnetic saturation phenomena which appeared in start-up and recycling phases and which were caused by the tightened operating condtions of pulse transformers with saturable cores had to be removed. Complex developent work led to relativly simple circuits which avoid saturation of pulse transformer cores for all observed conditions of operation.

4.4.2. The Power Control System.

The power control system, as described in the FIR |6| requires a response time of, approximately, ten full cycles of internal operation. At 50 kHz internal frequency, this corresponds to 200 μsec. in order to return to a condition of cyclic stability after occurence of an external disturbance. The actual time constant is estimated at 0.1 msec.

The improvement vs. the preceeding 20 kHz unit is, primarily, due to the increased internal frequency. An internal time constant of 0.1 msec. can be translated to a lower cut-off frequency f_c which can be no more than a tenfold of the inverse of the time constant: that is

$$f_c \simeq 1/(10\ 0.1\ 10^{-3}) \simeq 1 \text{ kHz} \qquad (4.78)$$

The above indicated cut-off frequency appeared well suited for the purpose at hand, especially for meeting the audio susceptibility requirements |12|.

The principles of the control electronics are described in the FIR and in the literature |2,6,12|.

One added protective feature is a current amplitude "clipper" which limits the absolute maximum of any current amplitude to a preset value. This

"clipper" is requisite to the use of transistors in series resonant circuits. Unlike the thyristor, is the transistor "unforgiving" whenever the rated maximum current is exceeded, even if momentary. The described protection feature is, therefore, an absolute necessity for the successful operation of series resonant cricuits which are being switched by transistors.

4.5. Limitations.

Certain limitations are inherent in the here presented approach. Some of these limitations are rooted in certain aspects of the applied functional philosophy; others find their causes in specific properties of the used materials and their available geometric configurations.

4.5.1. Limitations of the Functional Philosophy.

The expectations for a favorable efficiency of the presented converter are based on the ease with which the power transistors should switch, as discussed with reference to figure 2.3.

Yet, the efficiency of the technique which was applied to gain control over the individual output channels, as explained with reference to figures 3.4 and 3.6, is limited to specific conditions of operation. The "average"

resonant current $|i_1|_{av}$ has to be geared at any time to supply the necessary power for the channel with the highest demand. The other three power transformers are placed in series with the one "highest demand" channel; they have to carry, by necessity, the same relativly high current in their primary windings. The output power in these other three channels is controlled by the application of temporary short circuits to the respective transformers, as discussed with reference to figures 3.5 and 3.6.

The described method proves to be effective in terms of satisfaction of the control requirments. Yet, the efficiency of the system cannot equal that of a single channel system, when the processed power differs from a chosen design condition.

The alternative would be another approach in which the individual power transformers are placed in parallel and are being individually controlled. Pusuit of such an approach appeared not possible within the time limitations of this program.

4.5.2. Physical Limitations of Components.

Presently available materials and components are only marginally suited for the efficient processing of power at sizable currents with pulse frequencies in the order of 100 kHz.

Most of the components are intrinsically suited for these frequencies; this includes the semiconductor parts - the chips - of switching components. Appreciable difficulties arise with the connecting terminals of components, wires, switches and connectors which are not built to carry and transfer currents at levels of tens of Amperes, efficiently, with pulse frequencies near $2 \times 50\ 10^3 = 100$ kHz.

More will be said concerning this topic in the dicussion in subsection 5.2. At this time it is emphasized that all transfer of charge should move through Litz-wire or a similar structure in an almost uninterrupted circuit. This includes the access to the actual functional elements of components, such as the extended foils of the power capacitors, the chips of semiconductor components and, above all, the points of junctures, i.e., connectors, power switches and joining points.

It is, briefly, said here that the just described requirements are not beyond the existing technology. Yet, these features are not embodied in currently produced components and materials, as there was no demand for it.

5. Results.

System test data are presented in this section, followed by their interpretation in the form of a discussion.

5.1. System Test Data.

The system was tested in compliance with the Techical Guidelines. A variable and controllable voltage source in the form of a controllable, regulated dc power supply was used, which included the range of 22 to 32 VDC, to provide the needed input power. The individual output channels were loaded with resistors of appropriate electric and physcial dimmensions for adequate power dissipation capability.

Specifically:

$$R_{L1} = R_{L2} = 0.5 \text{ Ohm;} \tag{5.1}$$

$$R_{L3} = R_{L4} = 5 \text{ Ohm} \tag{5.2}$$

for full power operation. Switching resistor banks were used to perform the tests at the various levels of loading. Each of these resistors was capable to dissipate up to 50 Watts in still air.

The readings which were obtained with passive type, high frequency watt-

meters (Marek, Bremen; 0 - 100 kHz) were compared and reconciled with the readings of volt- and amperemeters with cut-off frequencies of 500 kHz.

The output voltages v_{oi} appeared to vary monotonically as functions of the input voltage e_s and the degree of loading $R_{Li}/R_{Li\ nom}$, where $R_{Li\ nom}$ is the nominal full load resistor for the ith output channel.

The output voltages v_{oi} (i = 1,2,3,4) are listed in Table 5.1 as functions of e_s and as functions of the extreme values of loading, i.e., $R_{Li}/R_{Li\ nom}$ = 1 and 10, respectivly. Recording of these test data appeared adequate to establish compliance of the system with the steady state requirements, as stipulated in the Technical Guidelines. This conclusion was derived from the above referred to monotonic behavior of the system in response to variation of the input voltage and of loading.

An inspection of the results in Table 5.1 shows that the data for any of the four channels is representative for the other three, as being well within the regulation requirements of $\pm$ 0.5 percent, or 2 percent, respectivly.

The data for the first output channel, $v_{o1} = 5\ V_{nom}$ is shown in graphic form in figure 5.1 to provide a pictorial presentation of the system's regulation characteristics. It is seen that the maximum deviation of v_{o1}

TABLE 5.1

Voltages v_{oi} of Output Channels as Functions of the Input Voltage e_s and of Full and Ten Percent Loading.

v_{oi}	v_{o1}		$-v_{o2}$		v_{03}		$-v_{o4}$	
$R_L/R_{L\ nom}$	10	1	10	1	10	1	10	1
e_s								
22	5.013	5.009	5.007	5.001	15.25	15.23	15.37	15.35
24	5.016	5.012	5.009	5.001	15.26	15.23	15.40	15.34
26	5.017	5.013	5.010	5.004	15.26	15.24	15.41	15.36
28	5.017	5.013	5.010	5.004	15.26	15.24	15.40	15.36
30	5.017	5.013	5.010	5.004	15.27	15.24	15.40	15.37
32	5.018	5.014	5.011	5.005	15.26	15.25	15.38	15.37

from its average value, given by

$$\tfrac{1}{2}(v_{o1\ max} - v_{o1\ min})/\tfrac{1}{2}(v_{o1\ max} + v_{o1\ min}) \simeq 9\ 10^{-4} = \Delta_1 \qquad (5.3)$$

or

$$100\ \Delta_1 = (100)(9\ 10^{-4}) = 0.09 \text{ percent} \qquad (5.4)$$

Likewise are:

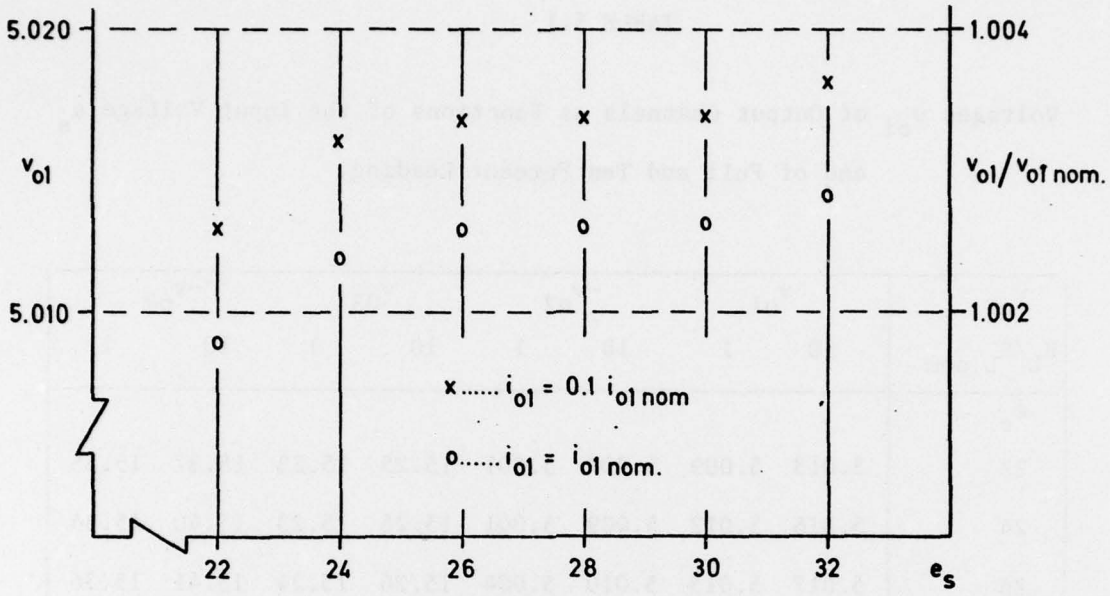

Figure 5.1.

Regulation of the 5 V output channel as function of e_s and $R_{L1}/R_{L1\ nom}$.

$$100\ \Delta_2 = (100\ )(10^{-3} = 0.1 \text{ percent} \tag{5.5}$$

$$100\ \Delta_3 = (100)(.98\ 10^{-3}) = 0.1 \text{ percent} \tag{5.6}$$

$$100\ \Delta_4 = (100)(.98\ 10^{-3}) = 0.1 \text{ percent} \tag{5.7}$$

An efficiency of 73.35 percent was established for the nominal operating point, at full power in the four output channels, when powered from a 28 Volt dc source. The complete data for this purpose are given in Table 5.3.

Table 5.2.

Currents i_{oi} in the Output Channels as Functions of the Input Voltage e_s and of Full and Ten Percent Loading.

i_{oi}	i_{o1}		i_{o2}		i_{o3}		i_{o4}	
$R_L/R_{L\ nom}$	10	1	10	1	10	1	10	1
e_s								
22	1.013	10.04	1.018	10.07	.3032	3.028	.3042	3.028
24	1.014	10.05	1.018	10.08	.3034	3.038	.3044	3.038
26	1.014	10.05	1.018	10.08	.3034	3.030	.3044	3.040
28	1.014	10.05	1.018	10.08	.3034	3.030	.3044	3.040
30	1.014	10.05	1.018	10.08	.3034	3.030	.3044	3.042
32	1.014	10.07	1.019	10.08	.3034	3.032	.3044	3.042

The peak to peak output voltage ripple voltages v_{ri} were viewed on an oscilloscope. Only qualitative and approximative readings appeared possible, because of common mode effects in the ac coupled differential amplifiers and the stray pick-up in the shielded probes. These effects were the results of attempts to view millivolt range signals. The shapes of these signals were those of somewhat distorted half-sinusoids, superimposed on a 60 Hz sine wave ripple, when viewed during the audio susceptibility test.

TABLE 5.3

Data for Calculation of the Converter's Efficiency

Under Nominal Operating Conditions.

	VDC	ADC	WATT	WATT
e_s	28.02			
i_s		9.424		
P_{in}				264.06
v_{o1}	5.013			
i_{o1}		10.05		
P_{o1}			50.381	
v_{o2}	-5.004			
i_{o2}		-10.08		
P_{o2}			50.440	
v_{o3}	15.24			
i_{o3}		3.03		
P_{o3}			46.177	

TABLE 5.3 (Continued)

	VDC	ADC	WATT	WATT
v_{o4}	-15.36			
i_{o4}		-3.04		
P_{o4}			46.694	
Sum of the P_{oi} (i = 1,2,3,4)				193.69

η_{28} = 100 193.69/264.06 = 73.35

The viewed peak to peak values related reasonably well to the rms content of these ripple voltages, as read by ac voltmeters with a bandwidth of 500 kHz.

A 60 Hz, 2.8 V_{rms} modulation signal was fed into the dc power supply-amplifier system. This signal was generated by a common audio-oscillator. The compounded effect caused by the 100 kHz converter operation and by the 60 Hz "moise" signal on the input voltage is summarized in Table 5.4.

TABLE 5.4.

Output Ripple Voltages v_{ri} of the Individual Output Channels for Full and for Ten Percent Loading.

mV_{rms}	v_{r1}		v_{r2}		v_{r3}		v_{r4}	
$R_L/R_{L\ nom}$	10	1	10	1	10	1	10	1
e_s								
22	7.18	4.98	7.68	5.38	15.26	12.34	15.47	12.51
24	7.24	5.02	7.76	5.42	15.35	12.46	15.56	12.63
26	7.30	5.10	7.82	5.52	15.44	12.61	15.65	12.78
28	7.34	5.16	7.88	5.56	15.56	12.70	15.78	12.87
30	7.42	5.22	7.94	5.62	15.66	12.78	15.88	12.95
32	7.52	5.28	8.02	5.70	15.79	12.91	15.99	13.07

Voltage overshoot of the individual channels was tested by sudden reduction of the respective loads from 100 to 10 percent. The corresponding overshoots were clipped near the 108 percent level of the nominal output voltages v_{oi}. The voltage clipping method which is applied for this purpose was described in subsection 3.2.4.

Current limiting of the individual channels near 105 percent of the respective full load currents was verified and found consistent with the intrinsic current source character of the described system |2,6|.

5.2. Discussion.

The test results indicate the feasibility of a rugged, ultra light dc converter. The low weight, or the high power density are rooted in the high internal frequency of operation at 50 kHz.

A power density of the components of 126 W/kg resulted from the construction of the breadboard. A power density of a packaged system of 80 W/kg can be projected if it is assumed that the packaging would add 60 percent to the component weight.

The system function performance complied with the goals, contained in the Technical Guidelines of 19 November 1974 (TGA), as recorded in the preceeding subsection 5.1.

The achieved efficiency of 73.35 % at full load is lower than the expected 80%. It was explained in subsection 2.3 with reference to (2.2) that the system efficiency could not exceed 81.2 percent even if no i^2R losses were involved at all in the system. The curve trace of the power dissipation

in one transistor, shown in figure 2.3 indicates that the loss in the switching transistors is solely restricted to the conduction losses and should be, therefore, independent of the frequency of operation. Once this assumption was verified, it remained to explain where the balance of dissipated power was being lost.

The dissipation plates of the semiconductor devices - transistors and rectifier diodes - were separate entities during the phase of development. The temperature of these devices indicated that the losses in these components were higher than those calculated. A closer scrutiny of these high frequency and fast recovery devices revealed that the thin external terminals are entirely inadequate for the intended purpose to carry up to 15 Amperes of current, not to speak of the rated 30 Amperes. This shortcoming appears quite plausible, because appreciable derating of the current which is actually conducted by these devices is mandatory in the conventional circuits which do not provide the absolute protection against current spikes. as does the presented system in which the switched current reaches 80% of the rated current in the steady state. These high speed and fast recovery devices have the almost fragile looks of the signal level transistors from which they have evolved over the years. A hockey-puck structure or some other suitable way of connecting the concerned chips to the high current circuits appears mandatory in order to construct efficient, low voltage converters. Other sources of ohmnic losses were found in the

area of joining of conductors and in the conducting structures themselves.

Banana plug connectors are dimensioned so that they could dissipate the heat that is being generated in them; less concern was devoted to the question of efficient power transfer. It appears, furthermore, mandatory to use at the frequency levels of 50 and 100 kHz Litz-wire everywhere: in the wire wound magnetic components and for the purspose of connecting components. Another problem area is that of joining wires. Litz wires cannot be joined at this time without creating volumes of conducting materials in which zones of thin depth of penetration would develop at 50 and 100 kHz.

Voltage drops which are due to contact potentials, whether soldered, crimped or pressure contacts are numerous in the described circuits. These potentials can develop individually the equivalent of milliohms of resistance, the order of magnitude of effective resistance of an entire magnetic device in the system.

The above described problem areas are not, necessarily, germane to the presented system. They will be found in any system that could sustain an efficient switching operation at the 50 kHz frequency level. Yet, the reslts which were obtained at the same internal frequency and with the same type of system |7| indicate that operation with substantially lower currents of 5 A_{av} at higher voltage levels, such as 220 VDC for 1 kW processed power can lead to the attainment of high efficiencies, such as 95%.

It can, therefor be said that the low power system at high current levels incorporate an intrinsic problem area which includes the joining technology and the physical structures of device terminals and the thereto pertaining internal connections. This problem area is seen as being distinct from the power losses due to switching phenomena for which the independence from the internal frequency of operation seems secured for the here presented system.

The limitations which were imposed by the lack of power Litz-wire and the other referred to problems associated with joints and component terminals surfaced clearly when the contruction of the model and the time schedule of the program had advanced to a point at which its completion in the presented form appeared necessary.

The applied principles of technology and the thereto pertaining circuitry have proven to be suited for operation in the 0 - 120 ^{o}F temperature environment with a reliability which exceeds 5000 hours MTBF |13|. Compliance with the requirements of electromagnetic compatibility should be attainable since the maximum rate of change of current is limited to $di/dt_{max} = \omega_o I_a \simeq 2\pi 60\ 10^3\ 20 \simeq 7.5$ A/µsec. This rate of change is substantially lower than the rate of rise of current of systems which switch comparable surrents forcibly in pulse width modulated systems at considerably lower internal frequencies of operation.

The development of technology to operate individually controlled loads in parallel with converters which employ series resonant circuits, would avoid the necessity to circulate the maximum resonant current i_1 at all times and thus enhance the converter's efficiency at lower levels of output power.

REFERENCES

1. Schwarz, F.C., Power Processing, NASA SP-244, 1971.

2. Schwarz, F.C., "An improved method of resonant current pulse modulation for power converters," IEEE Trans. IECI - 23, No. 2, May 1976.

3. Biess, J., Inouye, L., and Schoenfeld, A.D., "Thyristor power processor for the 30 cm mercury electric propulsion engine," AIAA Paper 15-433, 11th Electronic Propulsion Conference, New Orleans, 1975.

4. Cronin, D.L., Power Supply PP-6418( )/U, Technical Report, ECOM-0245-F, TRW Systems, OSD, March 1971.

5. Schwarz, F.C., "Electronic control system for efficient transfer of power through resonant circuits," U.S. Patent, No. 3,953,779, April, 1976.

6. Schwarz, F.C., Advanced Power Processing Techniques for DC to DC Converters, ECOM-74-0568-1, April, 1976.

7. Schwarz, F.C. and Klaassens, J.B., "A 95 percent efficient 1 kW dc converter with an internal frequency of 50 kHz," 8th IEEE-PESC, San Francisco, June, 1977.

8. Wilson, T.G., and Lee, F.C.Y., "Voltage spike analysis for a free running parallel inverter," IEEE Trans., MAG-10, No.3, pp. 969-972, September, 1972.

9. Schwarz, F.C. and Voulgaris, N.C., "A wide-band wattmeter for the measurement and analysis of power dissipation in semiconductor switching devices," IEEE Trans., ED-17. No. 9, September 1970.

10. Schwarz, F.C, "A method of resonant current pulse modulation for power converters," IEEE Trans. IECI-17, No. 2, May, 1970.

11. Schwarz, F.C., "A time domain analysis of the power factor for a rectifier filter system with over- and sub-critical inductance," IEEE Trans. IECI-20, No. 2, May, 1973.

12. Schwarz, F.C., Engineering Information on an Analog Signal to Discrete Time Interval Converter, NASA CR-134544, June, 1974.

DISTRIBUTION LIST
FINAL REPORT
CONTRACT NO. DAAB07-74-C-0568

COMMANDER
US ARMY ELECTRONICS R&D COMMAND
FORT MONMOUTH, NJ 07703

1 DELET-DD
2 DELET-DT
1 DELET-P
1 DELSD-L Tech Lib)
16 DELET-PE (J.Angello)

COMMANDER
US ARMY COMMUNICATIONS R&D COMMAND
FORT MONMOUTH, NJ 07703

1 USMC-LNO

COMMANDER
US ARMY COMMUNICATIONS & ELECTRONICS
MATERIEL READINESS COMMAND
FORT MONMOUTH, NJ 07703

2 DRESL-MS-TI

NASA SCIENTIFIC & TECH INFO FACILITY
BALTIMORE/WASHINGTON INTL AIRPORT
PO BOX 8757, MD 21240 1

CDR, US ARMY RESEARCH OFFICE
ATTN: DRXRO-IP
PO BOX 12211
RESEARCH TRIANGLE PARK, NC 27709 1

CDR, US ARMY SIGNALS WARFARE LAB
ATTN: DELSW-OS
ARLINGTON HALL STATION
ARLINGTON, VA 22212 1

COMMANDER
US ARMY MOBILITY EQP RES & DEV CMD
ATTN: DRXFB-R
FORT BELVOIR, VA 22060 1

HQDA(DAMA-ARZ-D)/Dr. F.D. VERDERAME
WASHINGTON, D.C. 20310 1

CDR, HARRY DIAMOND LABORATORIES
ATTN: LIBRARY
2800 POWDER MILL ROAD
ADELPHI, MD 20783 1

HQ ESD (DRI)
L.G. Hanscom AFB
BEDFORD, MA 01731 1

DEFENSE DOCUMENTATION CENTER
ATTN: DDC-TCA
CAMERON STATION (BLDG5)
ALEXANDRIA, VA 22314 1

COMMANDER
NAVAL ELECTRONICS LABORATORY CENTER
ATTN: LIBRARY
SAND DIEGO, CA 92152 1

CDR, NAVAL SURFACE WEAPONS CENTER
WHITE OAK LABORATORY
ATTN: LIBRARY, CODE WX-21
SILVER SPRING, MD 20910 1

COMMANDANT, MARINE CORPS
HQ, US MARINE CORPS
ATTN: CODE LMC
WASHINGTON, DC 20380 1

ROME AIR DEVELOPMENT CENTER
ATTN: DOCUMENTS LIBRARY (TILD)
GRIFFISS AFB, NY 13441 1

Mr. Donald Mortel
AF Aero Propulsion Lab. 1
Attn.: AFAPL-POE-1
Wright-Patterson AFB, Ohio 45433

Mr. Richard E. Oderwald 1
Department of the Navy
Hqs., US Marine Corps
Code LMC 4
Washington, DC 20380

Commander
Harry Diamond Laboratories
Attn.: DELHD-RDD (Mr. A. Benderly)
2800 Powder Mill Road
Adelphi, MD 20783 1

Power Information Center
University City Science Center
3624 Science Center
Philadelphia, PA 19104 1

Joseph B. Heckl
Naval Surface Weapon Center
White Oak Laboratory
Code WA - 13
Silver Spring, MD 20910 1

Leopold J. Johnson
Naval Electronics Lab Center
Code 4300
271 Cataline Blvd.
San Diego, CA 92152 1

Jerrold Foutz
Advanced Mechanization Appl. Div.
Naval Electronics Lab Center
271 Catalina Blvd.
San Diego, CA 92152 1

Richard L. Verga
AF Aeropropulsion Lab
Attn: AFAPL/POD-1
Wright Patterson AFB, OH 45433 1

R.D. Middlebrook, California
Institute of Technology
Pasadena, CA 91125 1

Thomas G. Wilson
College of Engineering
Duke University
Durham, NC 27706 1

Lawrence L. Ogborn
Purdue University
Lafayette, IN 47906 1

S.J. Lindema
Electro Optical Systems
Xerox Corporation
300 N. Halstead St.
Pasadena, CA 91107 1

A.D. Schoenfeld
TRW Inc. Systems Group
One Space Park
Redondo Beach, CA 90278 1

Don Lipke
Biometrics Instrument Corp.
55 North Fifth Street
Garland, TX 75040 1

William B. Collins
Martin Marietta Corp.
PO Box 179
Denver, CO 80201 1

Harry Linden
Engineerd Magnetics Div.
of Gulton Industries
13041, CA 90250 1

E. Towson Moore
Wilmore Electronics Co. Inc.
PO BOX 2973
West Durham, NC 27706 1

Paul Pittman
Westinghouse Electric Corp.
Research Laboratory
Churchill Boro
Pittsburgh, PA 15235 1

M. Olds
DOD Project Manager
Mobile Electric Power
Attn.: DRCPM-MEP-TM
7500 Poacklick Rd.
Springfield, VA 22150 1

Pierre A. Thollot
NASA Lewis Research Center
Attn.: MS 54-4
21000 Brookpark Rd.
Cleveland, OH 44135 1

Richard R. Secunde
NASA Lewis Research Center
Attn.: MS 54-4
21000 Brookpark Road
Cleveland, OH 44135 1

Paul R. Miller
NASA HQ Code NE
600 Independence Avenue, SW
Washington, DC 20546 1

Thomas J. Williams
NASA Jet Propulsion Laboratory
MS 198-220
4800 Oak Grove Drive
Pasadena, CA 91103 1

Edward Pasciutti
Goddard Space Flight Center
Code 711.3
Greenbelt, MD 20771 1

David Bell, III
NASA Johnson SC
Code EP-52
Houston, TX 77058 1

Roy Lanier, Jr.
NASA Marhall SC
Code EC-12
Huntsville, Al 35812 1

Donald S. Beard
ERDA MS 6-234
Div of Controlled Nuclear Research
Washington, DC 20545 1

James B. Wilson
Naval Research Laboratory
Code 5210.3
Washington, DC 20375 1